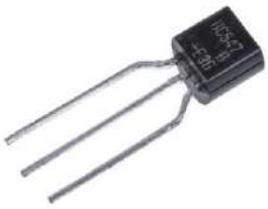
BASIC ELECTRONICS NOTES

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING



PREPARED BY

SMRUTIREKHA PRUSTY

MODULE I **(08 Hours)**

Introduction to Signals

Signals, Frequency and Time Domain analysis of signals, Elementary signals (impulse, step and ramp), Analog and digital signals, Discrete signals, Amplifiers, Digital logic inverter.

Operational Amplifiers

The Ideal Op Amp, Different stages of Op-Amp, Virtual Ground Concept Inverting and Non - Inverting configurations, Equivalent Circuit model, Op amp application in Integration, Differentiation and Summing Circuits.

Semiconductor Diodes

Introduction (Intrinsic, Extrinsic semiconductors and their energy level diagrams), P-N junction with open circuit, P-N junction with an applied voltage, Ideal diode, Characteristics of p-n Junction diodes, Rectifier circuits.

Special diodes- Zener diode and Light emitting diode. Display devices- Liquid Crystal Display, Seven Segment Display.

MODULE II **(10 Hours)**

Bipolar Junction Transistors (BJTs)

Simplified structure and physical operation of n-p-n and p-n-p transistors in the active region, Current-voltage characteristics of BJT (Common-Emitter, Common-Base and Common-Collector configurations).BJT as an amplifier and as a switch.

BJT Circuits at DC, Biasing in BJT amplifier circuits, Small Signal Operation of BJT: re-model, Simplified hybrid-π model and its application to single stage BJT amplifiers (Common- Emitter, Common-Base and Common-Collector configurations).A comparison on CB,CE and CC configuration.

Metal Oxide Semiconductor Field - Effect Transistors (MOSFETs)

Structure and Principle of operation of the Enhancement - Type and Depletion - Type MOSFETS. V - I Characteristics, DC - Biasing, Load – line and operating point.

MODULE III **(10 Hours)**

Digital Electronic Principles

Introduction, Binary digits, Logic levels and Digital waveforms, Introduction to basic logic operation, Number system, Decimal numbers, Binary numbers, Decimal-to-Binary conversion, Simple binary arithmetic.

Logic Gates and Boolean Algebra

The inverter, The AND, OR, NAND, NOR, Exclusive-OR and Exclusive-NOR gate, Boolean operations and expressions, Laws and Rules of Boolean algebra, DeMorgan's theorem, Boolean analysis of logic circuits, Standard forms of Boolean expressions, Boolean expression and truth table.

Text Books:

1. Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits", Oxford University Press, 7thEdition, 2014.
2. Thomas L. Floyd and R.P. Jain, "Digital Fundamentals", Pearson Education, 8thEdition, 2009.

Reference Books:

1. Thomas L. Floyd, Pearson Education, "Electronic Devices", Pearson Education, 7thEdition, 2005.
2. Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory", Pearson Education, 11thEdition, 2013.
3. Albert Malvono and David J. Bates, "Electronics Principles", Tata McGraw-Hill Publishing Company Limited, 7th Edition, 2007.

CHAPTER NAME **PAGE NO**

MODULE-I

ELECTRONICS

Electronics comprises the physics, engineering, technology and applications that deal with the emission, flow and control of electrons in vacuum and matter.This distinguishes it from classical electrical engineering as it uses active devices to control electron flow by amplification and rectification rather than just using passive effects such as resistance, capacitance and inductance.

INTRODUCTION TO SIGNAL

Electric signals (in electronics) – different voltages and currents in the electric network called electric "circuit" or "device", which can be further described as the process of changes a certain physical quantity or state of a physical object over certain period of time. **They are used for the purpose of visualization, registration and transmission of messages (information).** Signal can be a carrier of different information e.g. electric, magnetic and acoustic signals and contains the information parameter e.g. amplitude, frequency or pulse width. In electronics, the most important signals are the changes in electric charge, current, voltage and electromagnetic field. They are used to analyze the behavior of electronic circuits or to measure the changing electrical values.

What is Time Domain Analysis?

A time domain analysis is an analysis of physical signals, mathematical functions, or time series of economic or environmental data, in reference to time. Also, in the time domain, the signal or function's value is understood for all real numbers at various separate instances in the case of discrete-time or the case of continuous-time. Furthermore, an oscilloscope is a tool commonly used to see real-world signals in the time domain.

Moreover, a time-domain graph can show how a signal changes with time, whereas a frequency-domain graph will show how much of the signal lies within each given frequency band over a range of frequencies.

In general, when an analysis uses a unit of time, such as seconds or one of its multiples (minutes or hours) as a unit of measurement, then it is in the time domain. However, whenever an analysis concerns the units like Hertz, then it is in the frequency domain.

Frequency Domain

In physics, electronics, control systems engineering, and statistics, the **frequency domain** refers to the analysis of mathematical functions or signals with respect to frequency, rather than time. Put simply, a time-domain graph shows how a signal changes over time, whereas a frequency-domain graph shows how much of the signal lies within each given frequency band over a range of frequencies. A frequency-domain representation can also include information on the phase shift that must be applied to each sinusoid in order to be able to recombine the frequency components to recover the original time signal.

A given function or signal can be converted between the time and frequency domains with a pair of mathematical operators called transforms. An example is the Fourier transform, which converts a time function into a sum or integral of sine waves of different frequencies, each of which represents a frequency component. The "spectrum" of frequency components is the frequency-domain representation of the signal. The inverse Fourier transform converts the frequency-domain function back to the time function. A spectrum analyzer is a tool commonly used to visualize electronic signals in the frequency domain.

How is Time Domain Analysis Different from Frequency Domain?

Frequency domain is an analysis of signals or mathematical functions, in reference to frequency, instead of time. As stated earlier, a time-domain graph displays the changes in a signal over a span of time, and frequency domain displays how much of the signal exists within a given frequency band concerning a range of frequencies. Also, a

frequency-domain representation can include information on the phase shift that must be applied to each sinusoid to be able to recombine the frequency components to recover the original time signal.

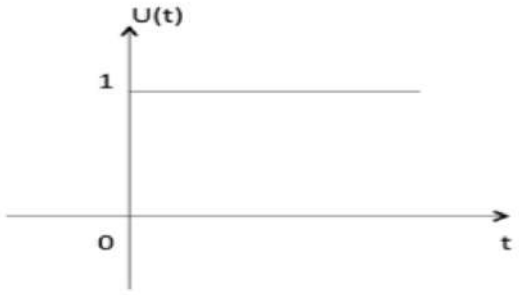
Furthermore, you can convert a designated signal or function between the frequency and time domains with a pair of operators called transforms. Moreover, a perfect example of a transform is the **Fourier transform**. Which converts a time function into an integral of sine-waves of various frequencies or sum, each of which symbolizes a frequency component. The so-called spectrum of frequency components is the frequency-domain depiction of the signal. However, as the name implies, the inverse Fourier transform converts the frequency-domain function back to the time function.

Elementary signals:

The elementary signals are used for analysis of systems. Such signals are,1. Step 2.Impulse 3. Ramp 4.Exponential 5.Sinusoidal

Unit Step Function

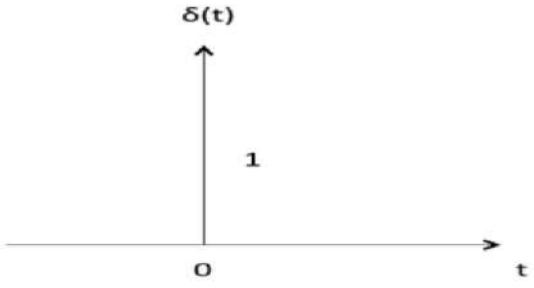
Unit step function is denoted by u(t). It is defined as u(t) = $\begin{cases} 1 & t \geqslant 0 \\ 0 & t < 0 \end{cases}$



- It is used as best test signal.
- Area under unit step function is unity.

Unit Impulse Function

Impulse function is denoted by δ(t). and it is defined as δ(t) = $\begin{cases} 1 & t = 0 \\ 0 & t \neq 0 \end{cases}$

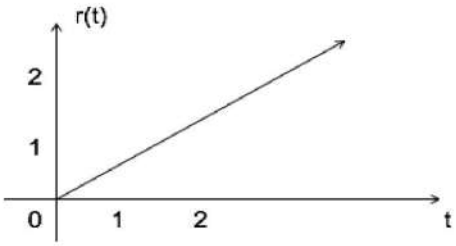


$$\int_{-\infty}^{\infty} \delta(t)dt = u(t)$$

$$\delta(t) = \frac{du(t)}{dt}$$

Ramp Signal

Ramp signal is denoted by r(t), and it is defined as r(t) = $\begin{cases} t & t \geqslant 0 \\ 0 & t < 0 \end{cases}$



$$\int u(t) = \int 1 = t = r(t)$$

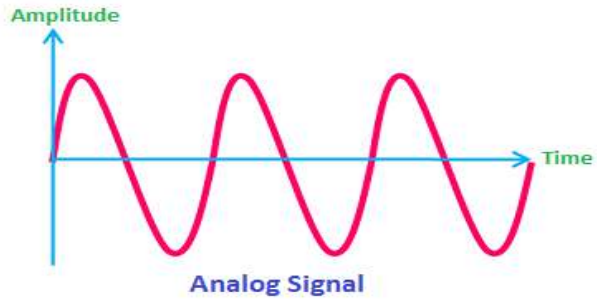
$$u(t) = \frac{dr(t)}{dt}$$

Area under unit ramp is unity.

ANALOG SIGNAL

An **analog signal** is a continuous wave denoted by a sine wave (pictured below) and may vary in signal strength (amplitude) or frequency (waves per unit time). The sine wave's amplitude value can be seen as the higher and lower points of the wave, while the frequency value is measured in the sine wave's physical length from left to right.

There are many examples of analog signals around us. The sound from a human voice is analog, because sound waves are continuous, as is our own vision, because we see various shapes and colors in a continuous manner due to light waves. Even a typical kitchen clock having its hands moving continuously can be represented as an analog signal.

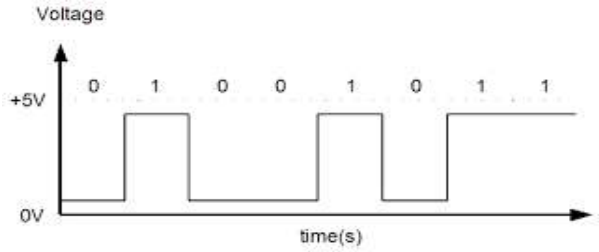


DIGITAL SIGNAL:

A **digital signal** is a signal that is being used to represent data as a sequence of discrete values; at any given time it can only take on one of a finite number of values. This contrasts with an analog signal, which represents continuous values; at any given time it represents a real number within a continuous range of values.

Simple digital signals represent information in discrete bands of analog levels. All levels within a band of values represent the same information state. In most digital circuits, the signal can have two possible values; this is called

a **binary signal** or **logic signal**. They are represented by two voltage bands: one near a reference value (typically termed as *ground* or zero volts), and the other a value near the supply voltage. These correspond to the two values "zero" and "one" (or "false" and "true") of the Boolean domain, so at any given time a binary signal represents one binary digit (bit).



Difference between analog and digital signals

S. No.	Analog signal	Digital Signal
1	Analog signals are continuous signals	Digital signals are discrete signals.
2	Analog signal uses continuous values for representing the information.	A digital signal uses discrete values for representing the information.
3	Analog signals can be affected by the noise during the transmission.	Digital signals cannot be affected by the noise during transmission.
4	Accuracy of Analog signal is affected by the noise.	Digital signals are noise-immune hence there accuracy is less affected
5	Devices which are using analog signals are less flexible	Device using digital signals are very flexible
6	Analog signals consumes less bandwidth	Digital signals consume more bandwidth.
7	Analog signal are stored in the form of continuous wave form.	Digital signals are stored in the form of binary bits "0", "1".
8	Analog signals have low cost.	Digital signals have high cost.
9	Analog signals are portable.	Digital signals are not Portable.
10	Analog signals give observation error	Digital Signals doesn't give observation error.

Continuous And Discrete Signals

Continuous-time signal:

Continuous-time signal is the "function of continuous-time variable that has uncountable or infinite set of numbers in its sequence".The continuous-time signal can be represented and defined at any instant of the time in its sequence. The continuous-time signal is also termed as analog signal. It is a continuous function of time defined on the real line (or axis) *R*. It has continuous amplitude and time. That is, the continuous-time signals will have certain value at any instant of time.

The continuous-time signal is drawn as shown in Figure 1 Shown below.

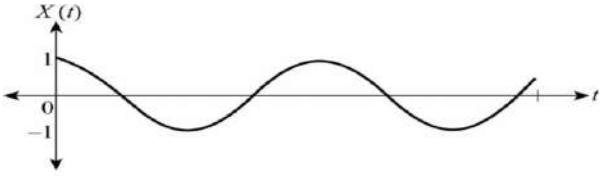


Figure 1

The examples for continuous-time signals are sine waves, cosine waves, triangular waves, and so on. The electrical signals also behave as continuous-time signals when these are derived in proportion with the physical parameters such as pressure, temperature, sound, and so on.

Discrete-time signal:

Discrete-time signal is the "function of discrete-time variable that has countable or finite set of numbers in its sequence". It is a digital representation of continuous-time signal.The discrete-time signal can be represented and defined at certain instants of time in its sequence. That is, the discrete-time signal is able to define only at the sampling instants. Digital signal can be obtained from the discrete-time signal by quantizing and encoding the sample values. The discrete-time signals are represented with binary bits and stored on the digital medium. The discrete-time signal is drawn as shown in Figure 2.

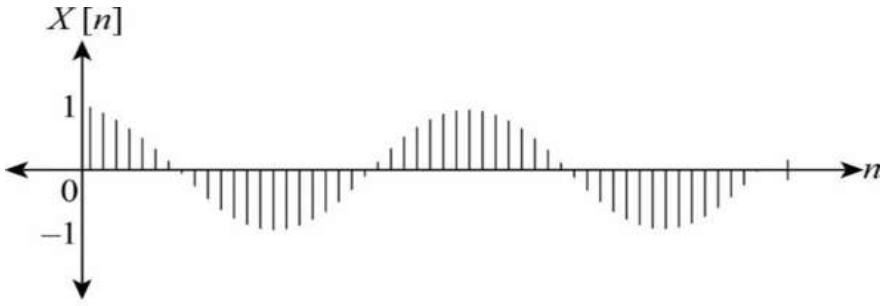


Figure 2

The output data from a computer is one of the examples of discrete-time signals.

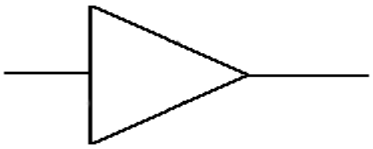
SAMPLING

In **signal** processing, **sampling** is the reduction of a continuous-time **signal** to a discrete-time **signal**. A common example is the conversion of a sound wave (a continuous **signal**) to a sequence of samples (a discrete-time **signal**). A **sample** is a value or set of values at a point in time and/or space.

AMPLIFIER

An **amplifier**, **electronic amplifier** or (informally) **amp** is an electronic device that can increase the power of a signal (a time-varying voltage or current). It is a two-port electronic circuit that uses electric power from a power supply to increase the amplitude of a signal applied to its input terminals, producing a proportionally greater amplitude signal at its output. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output voltage, current, or power to input. An amplifier is a circuit that has a power gain greater than one.

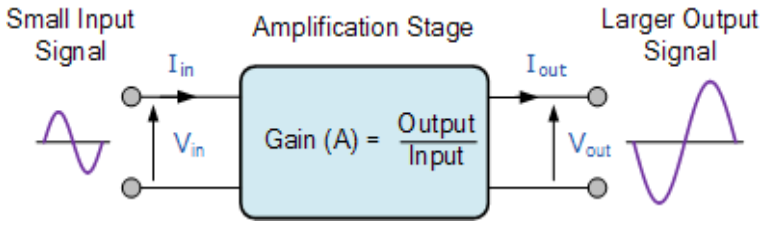
An amplifier can either be a separate piece of equipment or an electrical circuit contained within another device. Amplification is fundamental to modern electronics, and amplifiers are widely used in almost all electronic equipment. Amplifiers can be categorized in different ways. One is by the frequency of the electronic signal being amplified. For example, audio amplifiers amplify signals in the audio (sound) range of less than 20 kHz, RF amplifiers amplify frequencies in the radio frequency range between 20 kHz and 300 GHz, and servo amplifiers and instrumentation amplifiers may work with very low frequencies down to direct current.



Amplifier general symbol, used in system diagrams

Types of amplifiers:

- **A.F. Amplifiers**
- **I.F. Amplifiers**
- **R.F. Amplifiers**
- **Ultrasonic Amplifiers**
- **DC Amplifiers**
- **Operational Amplifiers**

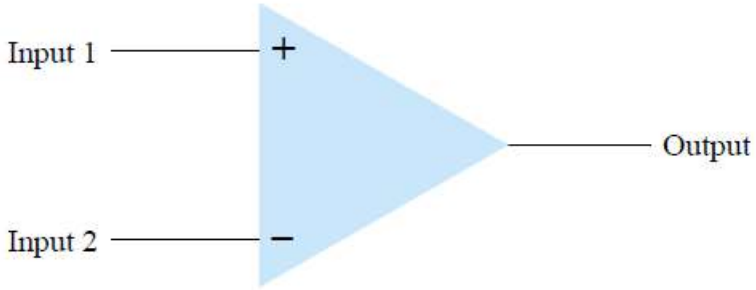


OPERATIONAL AMPLIFIER

An **operational amplifier** or **op amp** is a DC coupled voltage amplifier with a very high voltage gain.

Op amp is basically a multistage amplifier in which a number of amplifier stages are interconnected to each other in a very complicated manner. Its internal circuit consists of many transistors, FETs and resistors. All this occupies a very little space.
So, it is packed in a small package and is available in the Integrated Circuit (IC) form. The term **Op Amp** is used to denote an amplifier which can be configured to perform various operations like amplification, subtraction, differentiation, addition, integration etc. An example is the very popular IC 741.

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators,filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain. Figure given below shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. We call the terminal, marked with negative (-) sign as the inverting terminal and the terminal marked with positive (+) sign as the non-inverting terminal of the **operational amplifier**. If we apply an input signal at the inverting terminal (-) than the amplified output signal is 180^{o} out of phase concerning the applied input signal. If we apply an input signal to the non-inverting terminal (+) then the output signal obtained will be in phase, i.e
It will have no phase shift with respect to input signal. The op-amp also has two voltage supply terminals



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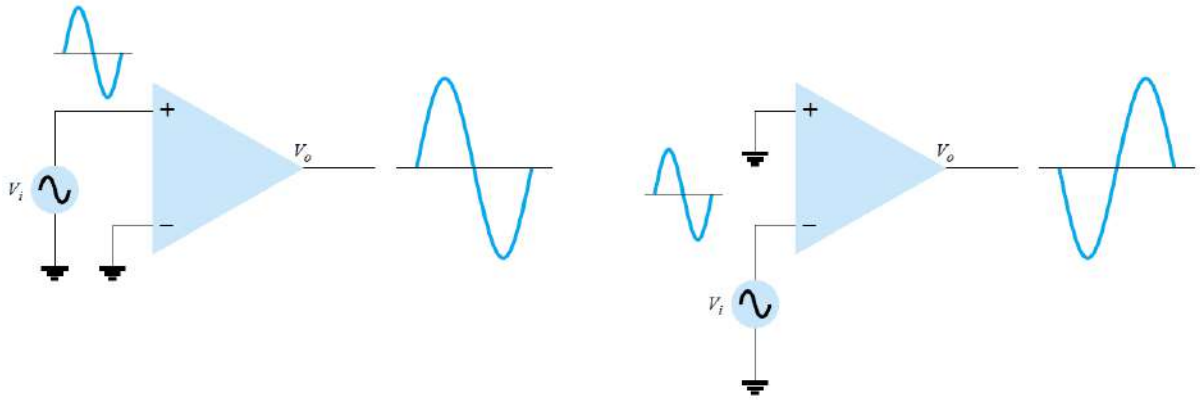
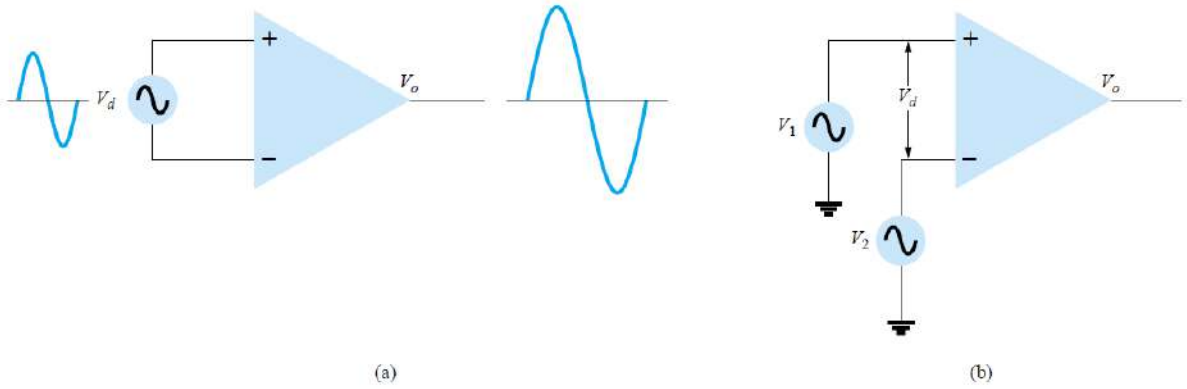
Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure below shows the signals connected.



Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure(a) below shows an input, *Va*, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure(b) below shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $Vi1 - Vi2$.



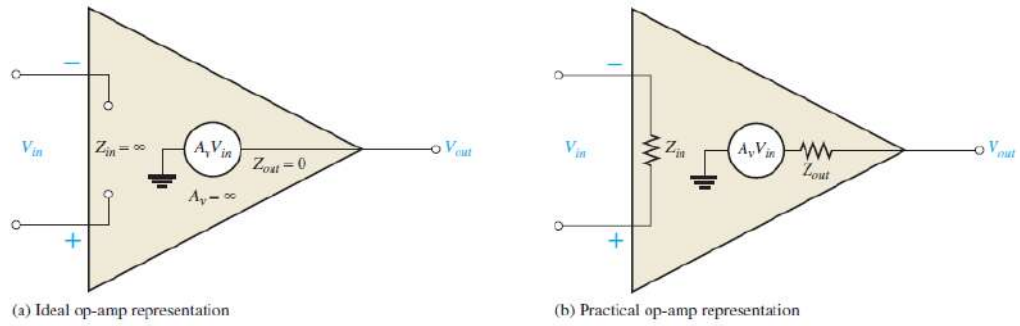
Ideal Op-Amp Characteristics

An ideal op-amp should have the following characteristics:

1. Infinite voltage gain (So that maximum output is obtained)
2. Infinite input resistance (Due to this almost any source can drive it)
3. Zero output resistance (So that there is no change in output due to change in load current)
4. Infinite bandwidth
5. Zero noise
6. Zero power supply rejection ratio (PSSR = 0)
7. Infinite common mode rejection ratio (CMMR = ∞)

Practical Operational Amplifier

None of the above-given parameters can be practically realized. A practical or real op-amp has some unavoidable imperfections and hence its characteristics differ from the ideal one. A real op-amp will have non-zero and non-infinite parameters.



(a) Ideal op-amp representation (b) Practical op-amp representation

Applications of Operational Amplifier

The integrated op-amps offer all the advantages of ICs such as high reliability, small size, cheap, less power consumption. They are used in variety of applications such as inverting amplifier and non inverting amplifiers, unity gain buffer, summing amplifier, differentiator, integrator, adder, instrumentation amplifier, Wien bridge oscillator, Filters etc.

Positiv Feedback ⇒ Oscillator

Negative Feedback ⇒ Amplifier

Working Principle of Op-Amp

Open Loop Operation of an Operational Amplifier

As said above an op-amp has a differential input and single ended output. So, if we apply two signals one at the inverting and another at the non-inverting terminal, an ideal op-amp will amplify the difference between the two applied input signals. We call this difference between two input signals as the differential input voltage. The

equation below gives the output of an operational amplifier. $V_{OUT} = A_{OL}(V_1 - V_2)$ Where, V_{OUT} is the voltage at the output terminal of the op-amp. A_{OL} is the open-loop gain for the given op-amp and is constant (ideally). For the IC 741 A_{OL} is 2 x 10^5.V_1 is the voltage at the non-inverting terminal. V_2 is the voltage at the inverting terminal. ($V_1 - V_2$) is the differential input voltage. It is clear from the above equation that the output will be non-zero if and only if the differential input voltage is non-zero (V_1 and V_2 are not equal), and will be zero if both V_1 and V_2 are equal. Note that this is an ideal condition, practically there are small imbalances in the op-amp. The open-loop gain of an op-amp is very high. Hence, an open loop operational amplifier amplifies a small applied differential input voltage to a huge value. Also, it is true that if we apply small differential input voltage, the operational amplifier amplifies it to a considerable value but this significant value at the output cannot go beyond the supply voltage of the op-amp. Hence it does not violate the law of conservation of energy.

Closed Loop Operation

The above-explained operation of the op-amp was for open-loop i.e. without a feedback. We introduce feedback in the closed loop configuration. This feedback path feeds the output signal to the input. Hence, at the inputs, two signals are simultaneously present. One of them is the original applied signal, and the other is the feedback signal. The equation below shows the output of a closed loop op-amp.

$$V_{OUT} = A_{CL}(V_1 - V_2) = A_{CL}V_D$$

Where V_{OUT} is the voltage at the output terminal of the op-amp. A_{CL} is the closed loop gain. The feedback circuit connected to the op-amp determines the closed loop gain $\mathbf{A_{CL}}$. $\mathbf{V_D = (V_1 - V_2)}$ is the differential input voltage. We say the feedback as positive if the feedback path feeds the signal from the output terminal back to the non-inverting (+) terminal. Positive feedback is used in oscillators. The feedback is negative if the feedback path feeds the part of the signal from the output terminal back to the inverting (-) terminal. We use negative feedback to the op-amps used as amplifiers. Each type of feedback, negative or positive has its advantages and disadvantages.

DIFFERENTIAL AND COMMONMODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i_1} - V_{i_2}$$

(non inverting terminal –inverting terminal)

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \frac{1}{2}(V_{i_1} + V_{i_2})$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-ofphase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c$$

where V_d = difference voltage
V_c =common voltage
A_d =differential gain of the amplifier
A_c =common-mode gain of the amplifier

Ideal Voltage Transfer Curve:

Ideal Voltage Transfer Curve – The ideal op-amp produces the output proportional to the difference between the two input voltages. The graphical representation of this statement gives the voltage transfer curve. It is the graph of output voltage $\mathbf{v_o}$ against the input Voltage $\mathbf{V_d}$ assuming gain constant. This graph is called **transfer** characteristics,of the op-amp.

Now the output voltage is proportional to difference input voltage but only upto the positive and negative saturation are specified by the manufacturer

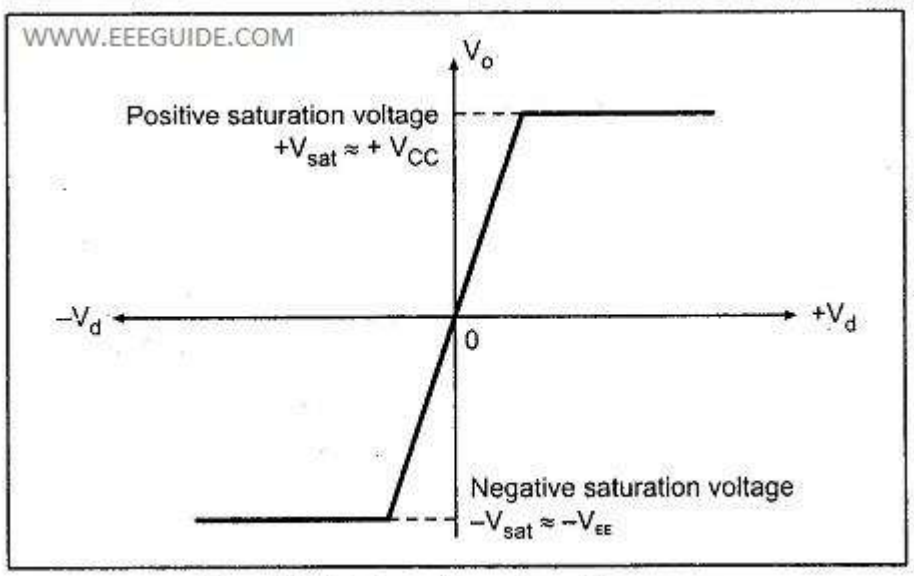
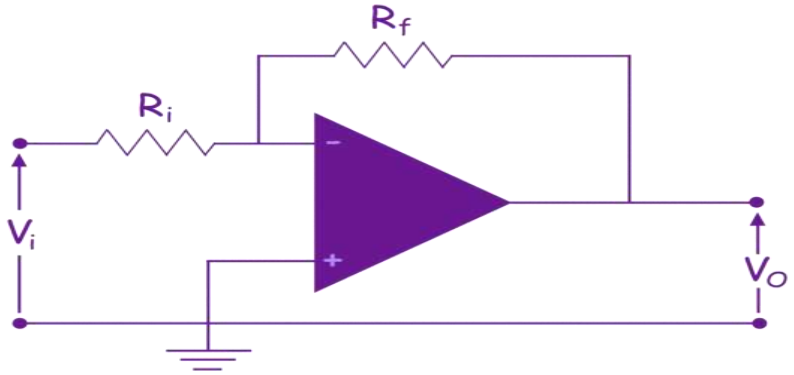


Fig. 2.7 Ideal voltage transfer curve

Thus note that the op-amp output voltage gets saturated at $+V_{cc}$ and $-V_{EE}$ and it can not produce output voltage more than $+V_{cc}$ and vEE. Practically saturation voltages $+V_{sat}$, and $-V_{sat}$ are slightly less than $+V_{cc}$ and $-V_{EE}$.Middle region is known as region of operation of OPAMP or linear region.

Negative Feedback in Op Amp

We obtain **Negative feedback in an op amp** by connecting output terminal of an op amp to its inverting input terminal through a suitable resistance as shown below.



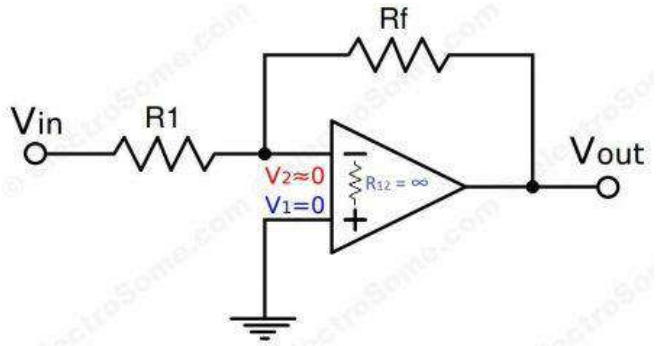
The gain of an op amp with negative feedback is called **closed loop gain**.

The use of negative feedback can significantly improve the performance of an operational amplifier and any op-amp circuit that does not use negative feedback is considered too unstable to be useful. But how can we use negative feedback to control an op-amp. Well consider the circuit below of a Non-inverting Operational Amplifier.

OPEN LOOP-NO FEEDBACK PATH(LESS STABLE)

CLOSED LOOP-FEEDBACK PATH(MORE STABLE)

Virtual Ground Concept – OPAMP



Using Infinite Voltage Gain

We already know that an ideal opamp will provide infinite voltage gain. For real opamps also the gain will be very high such that we can consider it as infinite for calculation purposes.

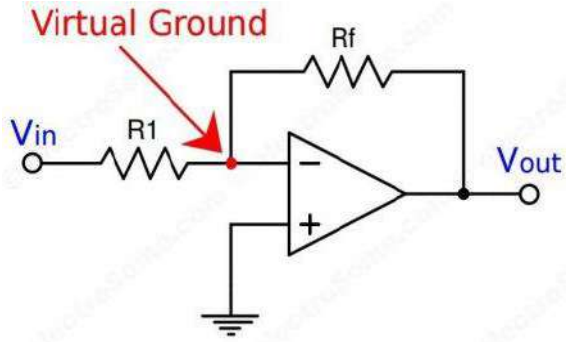
- **Gain = Vo/Vin**

As gain is infinite, **Vin = 0**

- Vin = V2 – V1

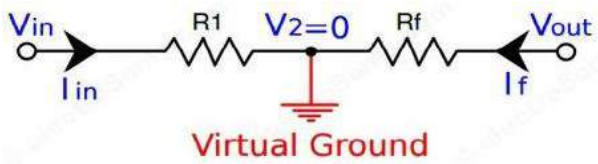
In the above circuit V1 is connected to ground, so V1 = 0. Thus V2 also will be at ground potential.

- **V2 = 0**



Why we need Virtual Ground ?

Virtual Ground concept is very useful in analysis of an opamp when negative feedback is employed. It will simply a lot of calculations and derivations.



Above concept is valid only when **negative feedback** is applied to opamp like in inverting ampliers.

Assumptions regarding OPAMP:(NEGATIVE FEEDBACK CLOSED LOOP OPAMP)

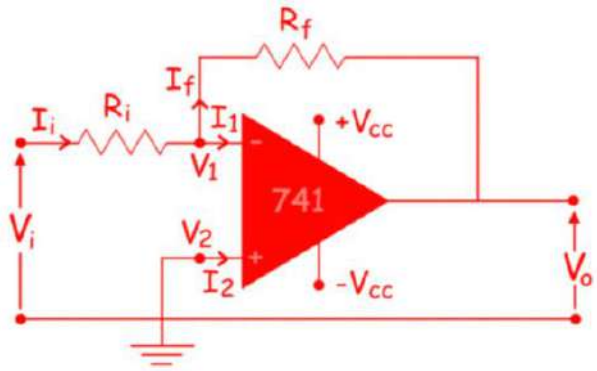
1.Current drawn by either of input terminals of opamp or current entering to opamp is zero as IDEAL OPAMP has infinite input impedance: $I_1 = I_2$

2.Voltage difference between two input terminal is zero. $V_d = V_1 - V_2 = 0$

Inverting Operational Amplifier | Inverting Op Amp

We call the operational amplifier as an inverting operational amplifier or an inverting op-amp when the op-amp circuit produces the output which is out of phase with respect to its input by 180°.

This means that if the input pulse is positive, then the output pulse will be negative and vice versa. The figure below shows an **inverting operational amplifier** built by using an op-amp and two resistors. Here we apply the input signal to the inverting terminal of the op-amp via the resistor R_i. We connect the non-inverting terminal to ground. Further, we provide the feedback necessary to stabilize the circuit, and hence to control the output, through a feedback resistor R_f.



Mathematically the voltage gain offered by the circuit is given as

$$A_v = \frac{V_o}{V_i}$$

Where, $V_i - V_1 = I_i R_i$ $V_1 - V_o = I_f R_f$ However, we know that an ideal op amp has infinite input impedance due to which the currents flowing into its input terminals are zero i.e. **$I_1 = I_2 = 0$. Thus, $I_i = I_f$.** Hence,

$$V_i - V_1 = I_f R_i$$

$$V_1 - V_o = I_f R_f$$

We also know that in an ideal op amp the voltage at inverting and non-inverting inputs are always equal. As we have grounded the non inverting terminal, zero voltage appears at the non inverting terminal. That means $V_2=0$.Hence,$V_1 = 0$, also. So, we can write

$$V_i - 0 = I_f R_i$$

$$0 - V_o = I_f R_f$$

From, above two equations, we get,

$$-\frac{V_o}{V_i} = \frac{I_f R_f}{I_f R_i} \Rightarrow \frac{V_o}{V_i} = -\frac{I_f R_f}{I_f R_i}$$

$$\Rightarrow \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

The voltage gain of the **inverting operational amplifier** or **inverting op amp** is,

$$A_v = -\frac{R_f}{R_i}$$

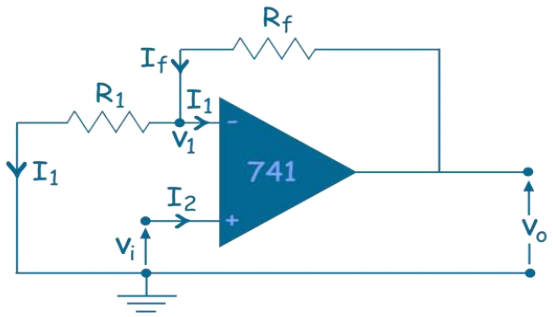
This indicates that the voltage gain of the inverting amplifier is decided by the ratio of the feedback resistor to the

input resistor with the minus sign indicating the phase-reversal. Further, it is to be noted that the input impedance of the inverting amplifier is nothing but **R_i**.
Inverting amplifiers exhibit excellent linear characteristics which make them ideal as DC amplifiers. Moreover, they are often used to convert input current to the output voltage in the form of Transresistance or Transimpedance Amplifiers. Further, these can also be used in audio mixers when used in the form of Summing Amplifiers.

Non Inverting Operational Amplifier | Non Inverting Op Amp

Non inverting amplifier is an op amp based amplifier with positive voltage gain.

A **non inverting operational amplifier** or **non inverting op amp** uses op amp as main element. The op amp has two input terminals (pins). One is inverting denoted with minus sign (-), and other is non-inverting denoted with a positive sign (+). When we apply any signal to the non – inverting input of, it does not change its polarity when it gets amplified at the output terminal. So, in that case, the gain of the amplifier is always positive.



Here, in the above circuit, we connect an external resistance R_1 and feedback resistance R_f at inverting input. Now, by applying Kirchhoff Current Law, we get,

$$\frac{v_1}{R_1} = \frac{v_o - v_1}{R_f} \ldots\ldots\ldots \quad (i)$$

Let us assume the input voltage applied to the non inverting terminal is v_i. Now, if we assume that the op amp in the circuit is ideal op amp, then,

$$v_1 = v_i$$

Therefore, equation (i) can be rewritten as,

$$\frac{v_i}{R_1} = \frac{v_o - v_i}{R_f}$$

$$\Rightarrow v_i \frac{R_f}{R_1} = v_o - v_i$$

$$\Rightarrow v_o = v_i \left(1 + \frac{R_f}{R_1}\right)$$

$$\Rightarrow \frac{v_o}{v_i} = \left(1 + \frac{R_f}{R_1}\right)$$

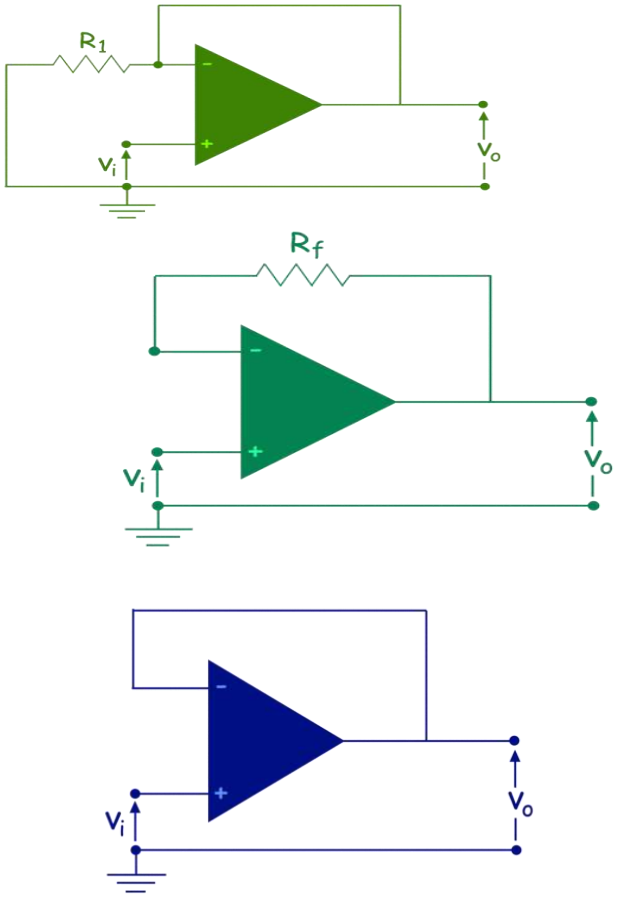
The closed loop gain of the circuit is,

$$A = \left(1 + \frac{R_f}{R_1}\right)$$

This term does not contain any negative part. Hence, it proves that the input signal to the circuit gets amplified without changing its polarity at the output.From the expression of voltage gain of an **non inverting op amp**, it is clear that, the gain will be unity when $R_f = 0$ or $R_1 \rightarrow$infinite.

$$When,\ R_f = 0$$
$$A = \left(1 + \frac{R_f}{R_1}\right) = \left(1 + \frac{0}{R_1}\right) = 1$$
$$When,\ R_1 \to \infty$$
$$A = \left(1 + \frac{R_f}{R_1}\right) = \left(1 + \frac{R_f}{\infty}\right) = 1$$

So, if we short circuit the feedback path and/or open the external resistance of the inverting pin, the gain of the circuit becomes 1.

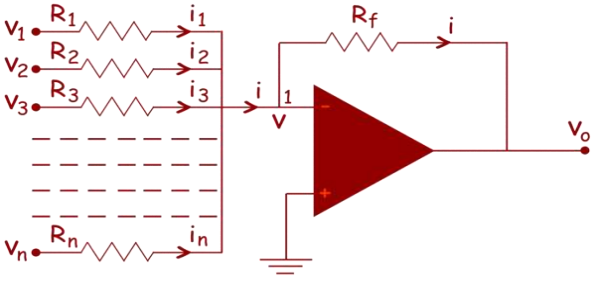


This circuit is called voltage follower or unity gain amplifier. This is used to isolate two cascaded circuits, because of its infinitely large impedance, at op amp inputs

APPLICATION OF OPAMP:

1. SUMMING AMPLIFIER

Summing amplifier is basically an op amp circuit that can combine numbers of input signal to a single output that is the weighted sum of the applied inputs. This simple inverting amplifier can easily be modified to **summing amplifier**, if we connect several input terminals in parallel to the existing input terminals as shown below.



Here, n numbers of input terminal are connected in parallel. Here, in the circuit, the non-inverting terminal of the op amp is grounded, hence potential at that terminal is zero. As the op amp is considered as ideal op amp,

the potential of the inverting terminal is also zero. So, the electric potential at node 1, is also zero. From the circuit, it is also clear that the current i is the sum of currents of input terminals.
Therefore,

$$i = i_1 + i_2 + i_3 + \cdots\cdots + i_n$$
$$\Rightarrow i = \frac{v_1 - 0}{R_1} + \frac{v_2 - 0}{R_2} + \frac{v_3 - 0}{R_3} + \cdots\cdots + \frac{v_n - 0}{R_n}$$
$$\Rightarrow i = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots\cdots + \frac{v_n}{R_n} \cdots\cdots (i)$$

Now, in the case of ideal op amp the current at the inverting and non-inverting terminal are zero. So, as per Kirchhoff Current Law, the entire input current passes through the feedback path of resistance R_f. That means,

$$i = \frac{0 - v_0}{R_f} = -\frac{v_0}{R_f} \cdots\cdots (ii)$$

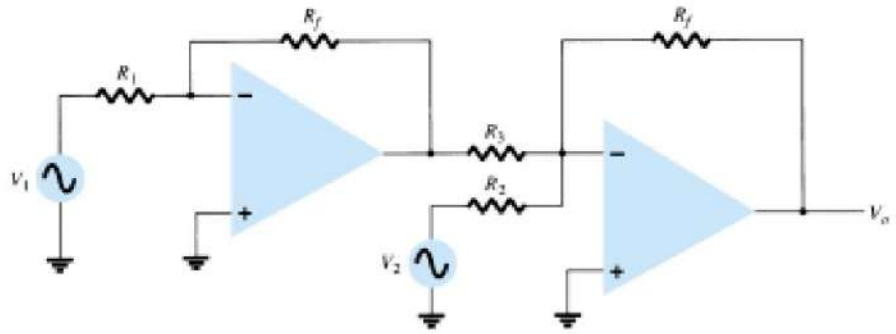
From, equation (i) and (ii), we get,

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots\cdots + \frac{v_n}{R_n} = -\frac{v_0}{R_f}$$
$$\Rightarrow v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3 + \cdots\cdots + \frac{R_f}{R_n}v_n\right)$$

This indicates that output voltage v_0 is weighted sum of numbers of input voltages.

2. DIFFERENCE AMPLIFIER OR OP AMP SUBTRACTOR:

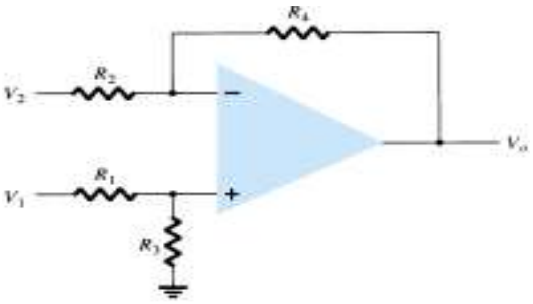
Two signals can be subtracted, one from the other, in a number of ways. Figure given below shows two op-amp stages used to provide subtraction of input signals. The resulting output is given by:



$$V_o = -\left[\frac{R_f}{R_3}\left(-\frac{R_f}{R_1}V_1\right) + \frac{R_f}{R_2}V_2\right]$$

$$\boxed{V_o = -\left(\frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1}V_1\right)}$$

Another connection(both signals applied to single opamp) to provide subtraction of two signals is shown in Fig. given below This connection uses only one op-amp stage to provide subtracting two input signals. Using superposition the output can be shown..

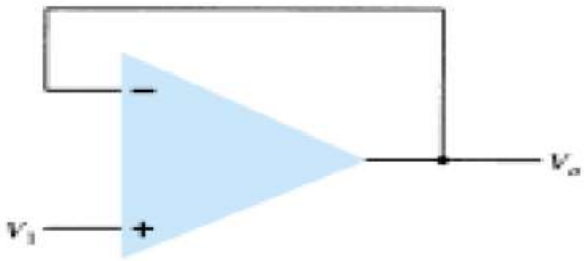


$$V_o = \frac{R_3}{R_1 + R_3}\frac{R_2 + R_4}{R_2} V_1 - \frac{R_4}{R_2} V_2$$

3. VOLTAGE BUFFER

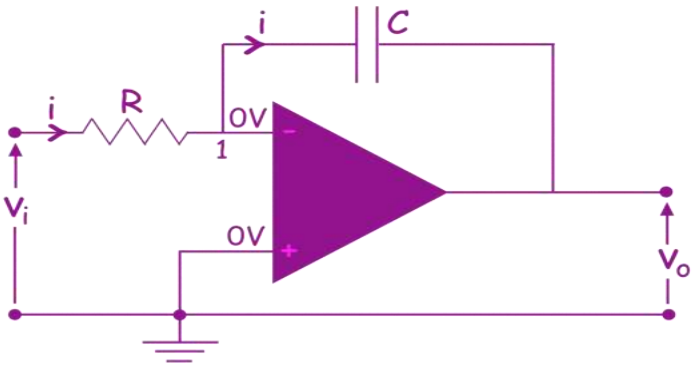
A voltage buffer circuit provides a means of isolating an input signal from a load by using a stage having unity voltage gain, with no phase or polarity inversion, and acting as an ideal circuit with very high input impedance and low output impedance. Figure given below shows an op-amp connected to provide this buffer amplifier operation. The output voltage is determined by

$Vo = V1$



4. **OP AMP AS INTEGRATOR**

op amp integrator circuit can be done, if we replace the feedback resistor $\mathbf{R_f}$ by a capacitor C as shown below.



In an ideal op amp the voltage at non inverting input terminal is same as that of inverting input.

Here, in the circuit, as the non inverting input is grounded, the electric potential of inverting input will also be zero as non inverting input. In an ideal op amp, no current entires to the op amp through both inverting and non inverting inputs.

Now, if we apply Kirchhoff current law at node 1 of the above circuit, shown in figure , we get,

$$\frac{v_i}{R} = -C\frac{dv_0}{dt}$$

$$\Rightarrow dv_0 = -\frac{1}{RC} v_i \, dt$$

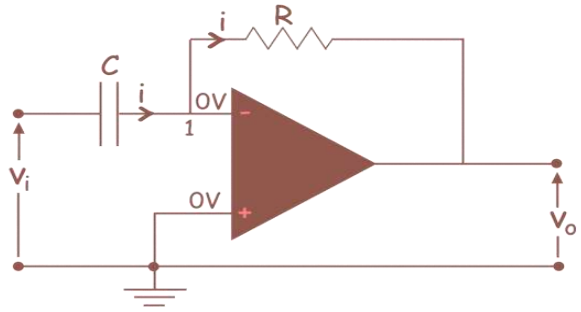
Integrating both side, we get,

$$v_0 = -\frac{1}{RC}\int v_i \, dt$$

This is the integral function of input voltage.

5. OP AMP DIFFERENTIATOR

Differentiator is an op amp based circuit, whose output signal is proportional to differentiation of input signal.An **op amp differentiator** is basically an inverting amplifier with a capacitor of suitable value at its input terminal. The figure below shows the basic circuit diagram of an **op amp differentiator**.



We will first assume that the op amp used here is an ideal op amp. We know that the voltage at both inverting and non inverting terminals of an ideal op amp is same. As the electric potential at non inverting terminal is zero since it is grounded. The electric potential of inverting terminal is also zero, as the opamp is ideal. Because, we know that the electric potential at non – inverting and inverting terminals. It is also known to us that the current entering through inverting and non inverting terminal of an ideal op amp is zero.
Considering, these conditions of an ideal op amp, if we apply Kirchhoff Current Law at node 1 of the **op amp differentiator circuit**, we get,

$$C\frac{dv_i}{dt} = -\frac{v_0}{R}$$

$$\Rightarrow v_0 = -RC\,\frac{dv_i}{dt}$$

The above equation shows that the output voltage is the derivative of the input voltage.

OPAMP PARAMETERS:

1.COMMON-MODE REJECTION RATIO

$$\text{CMRR} = \frac{A_d}{A_c}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR (log)} = 20 \log_{10}\frac{A_d}{A_c} \quad \text{(dB)}$$

$$V_o = A_d V_d + A_c V_c = A_d V_d\left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

we can write the above as

$$V_o = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d}\right)$$

2.INPUT OFFSET VOLTAGE :

The **input offset voltage** (V_{IO}) is a parameter defining the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier (op-amp), to make the output zero (for voltage amplifiers, 0 volts with respect to ground or between differential outputs. The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. An ideal op-amp amplifies the differential input; if this input difference is 0 volts (i.e. both inputs are at the same voltage), the output should be zero. However, due to manufacturing process, the differential input transistors of real op-amps may not be exactly matched. This causes the output to be zero at a non-zero value of differential input, called the input offset voltage. To determine the effect of this input voltage on the output, consider the connection shown in figure given below: Using $V_o = AV_i$, we can write:

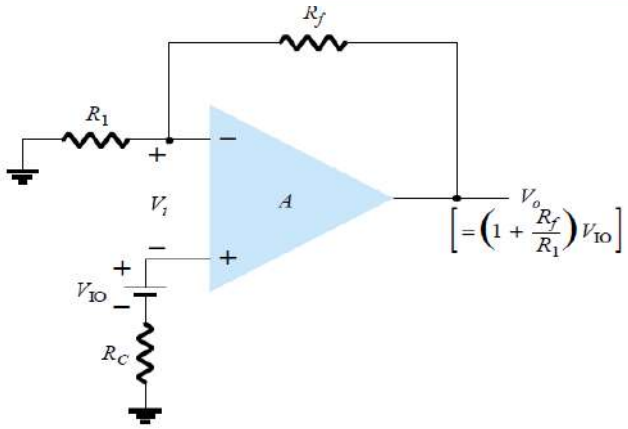
$$V_o = AV_i = A\left(V_{IO} - V_o \frac{R_1}{R_1 + R_f}\right)$$

Solving for V_o, we get

$$V_o = V_{IO} \frac{A}{1 + A[R_1/(R_1 + R_f)]} \approx V_{IO} \frac{A}{A[R_1/(R_1 + R_f)]}$$

from which we can write

$$V_o(\text{offset}) = V_{IO} \frac{R_1 + R_f}{R_1}$$



Equation shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

3.

INPUT BIAS CURRENT, I_{IB}

A parameter related to I_{IO} and the separate input bias currents I_{IB}^+ and I_{IB}^- is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^+ + I_{IB}^-}{2}$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB}. It can be shown that for $I_{IB}^+ > I_{IB}^-$

$$I_{\text{IB}}^{+} = I_{\text{IB}} + \frac{I_{\text{IO}}}{2}$$

$$I_{\text{IB}}^{-} = I_{\text{IB}} - \frac{I_{\text{IO}}}{2}$$

4.INPUT OFFSET CURRENT:

It is the algebraic difference between the currents into the noninverting and inverting terminals of OPAMP.

$$I_{\text{IO}} = I_{\text{IB}}^{+} - I_{\text{IB}}^{-}$$

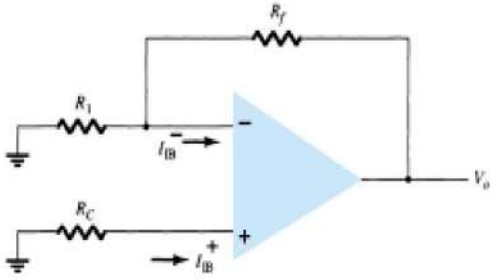
5.OUTPUT OFFSET VOLTAGE DUE TO INPUT OFFSET CURRENT:I_{IO}

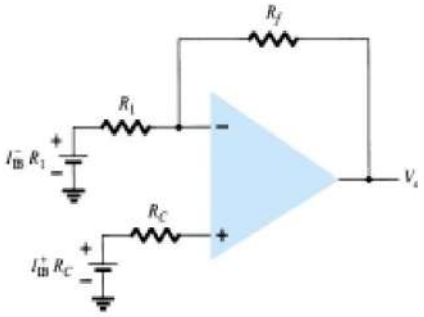
An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For typical op-amp connection, such as that shown in Fig., an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops, as shown in Fig., we can determine the expression for the resulting output voltage. Using superposition, the output voltage due to input bias current I_{IB}^{+},denoted by V_O^{+} is

$$V_o^{+} = I_{\text{IB}}^{+} R_C\left(1 + \frac{R_f}{R_1}\right)$$

while the output voltage due to only I_{IB}^{-}, denoted by V_o^{-}, is

$$V_o^{-} = I_{\text{IB}}^{-} R_1\left(-\frac{R_f}{R_1}\right)$$





for a total output offset voltage of

$$V_o(\text{offset due to } I_{\text{IB}}^{+} \text{ and } I_{\text{IB}}^{-}) = I_{\text{IB}}^{+} R_C\left(1 + \frac{R_f}{R_1}\right) - I_{\text{IB}}^{-} R_1 \frac{R_f}{R_1}$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{IO} = I_{IB}^{+} - I_{IB}^{-}$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (14.17) we can write

$$V_o(\text{offset}) = I_{IB}^{+}(R_1 + R_f) - I_{IB}^{-} R_f$$

$$= I_{IB}^{+} R_f - I_{IB}^{-} R_f = R_f (I_{IB}^{+} - I_{IB}^{-})$$

resulting in

$$V_o(\text{offset due to } I_{IO}) = I_{IO} R_f$$

TOTAL OFFSET DUE TO V_{IO} AND I_{IO}

Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to } V_{IO})| + |V_o(\text{offset due to } I_{IO})|$$

6. GAIN–BANDWIDTH

Because of the internal compensation circuitry included in an op-amp, the voltage gain drops off as frequency increases. Op-amp specifications provide a description of the gain versus bandwidth. Figure given below provides a plot of gain versus frequency for a typical op-amp. At low frequency down to dc operation the gain is that value listed by the manufacturer's specification $\boldsymbol{A_{VD}}$ (voltage differential gain) and is typically a very large value. As the frequency of the input signal increases the open-loop gain drops off until it finally reaches the value of 1 (unity). The frequency at this gain value is specified by the manufacturer as the unity-gain bandwidth, B_1. While this value is a frequency (see Fig.)at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

Another frequency of interest is that shown in Fig. at which the gain drops by 3 dB (or to 0.707 the dc gain, $\boldsymbol{A_{VD}}$), this being the cutoff frequency of the op-amp, $\boldsymbol{f_C}$. In fact, the unity-gain frequency and cutoff frequency are related by

$$f_1 = A_{VD} f_C$$

Equation shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

7.SLEW RATE:

Another parameter reflecting the op-amp's ability to handling varying signals is slew rate, defined as

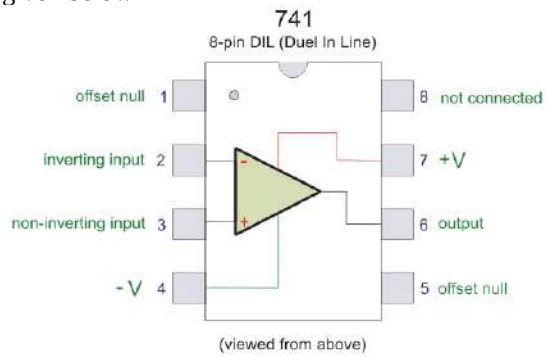
slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/μs)

$$\text{SR} = \frac{\Delta V_o}{\Delta t} \quad \text{V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate is exceeded.

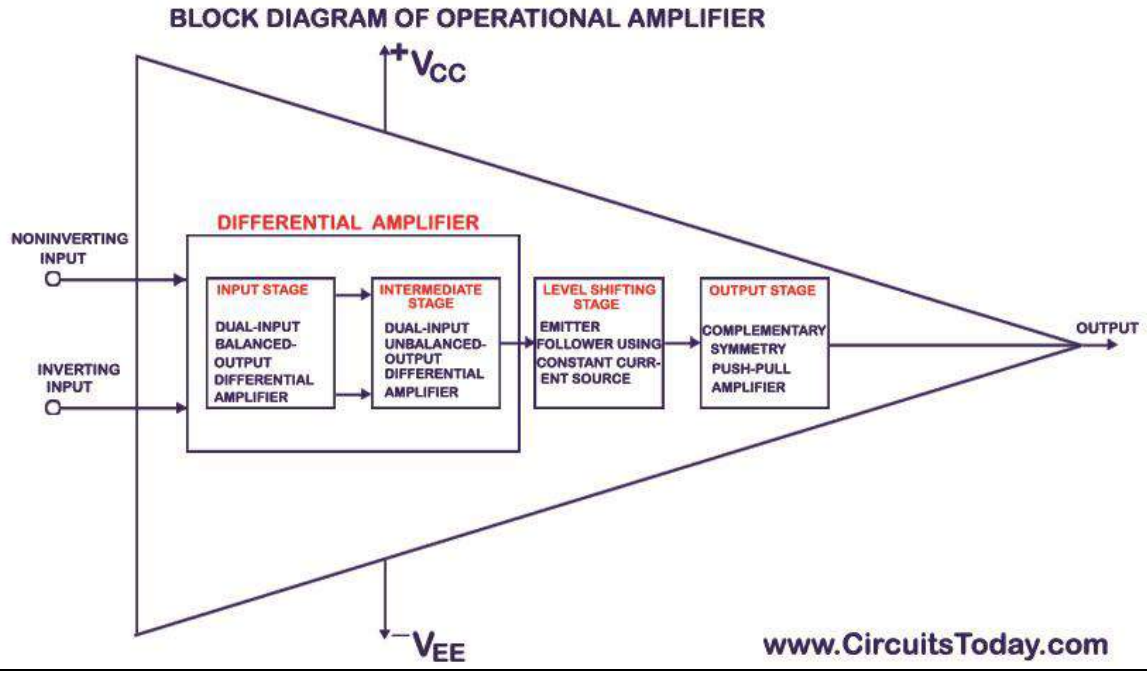
Pin Diagram of an Op Amp IC

The op amp IC we are going to discuss about here is IC 741. It is an 8 pin IC. The pin configuration of IC 741 is given below



PIN 1 – Offset Null
PIN 2 – Inverting input
PIN 3 – non- inverting input
PIN 4 – negative voltage supply
PIN 5 – offset null
PIN 6 – output
PIN 7 – positive voltage supply
PIN 8 – not connected

Block Diagram Of Operational Amplifier (Op-amp)



The op-amp begins with a differential amplifier stage, which operates in the differential mode. Thus the inputs noted with '+' & '- ' .

The positive sign is for the non-inverting input and negative is for the inverting input. The non-inverting input is the ac signal (or dc) applied to the differential amplifier which produces the same polarity of the signal at the output of op-amp. The inverting signal input is the ac signal (or dc) applied to the differential amplifier. This produces a 180 degrees out of phase signal at the output.

The inverting and non-inverting inputs are provided to the input stage which is a dual input, balanced output differential amplifier. The voltage gain required for the amplifier is provided in this stage along with the input resistance for the op-amp. The output of the initial stage is given to the intermediate stage, which is driven by the output of the input stage.

In this stage direct coupling is used, which makes the dc voltage at the output of the intermediate stage above ground potential. Therefore, the dc level at its output must be shifted down to 0Volts with respect to the ground. For this, the level shifting stage is used where usually an emitter follower with the constant current source is applied. The level shifted signal is then given to the output stage where a push-pull amplifier increases the output voltage swing of the signal and also increases the current supplying capability of the op-amp.

SEMICONDUCTOR DIODE:

Definition of Semiconductor

The materials that are neither conductor nor insulator with energy gap of about 1 eV (electron volt) are called semiconductors.

Most common materials commercially used as semiconductors are germanium (Ge) and silicon (Si) because of their property to withstand high temperature. That means there will be no significant change in energy gap with changing temperature.The relation between energy gap and absolute temperature for Si and Ge are given as,

$$E_g = 1.210 - 3.60 \times 10^{-4} \times T \quad eV \quad (for\ Si)$$

$$E_g = 0.785 - 2.23 \times 10^{-4} \times T \quad eV \quad (for\ Ge)$$

Where, T = absolute temperature in ^oK
Assuming room temperature to be 300^oK,

$$E_g = 1.210 - 3.60 \times 10^{-4} \times 300 \approx 1.1 \quad eV \quad (for\ Si)$$

$$E_g = 0.785 - 2.23 \times 10^{-4} \times 300 \approx 0.72 \quad eV \quad (for\ Ge)$$

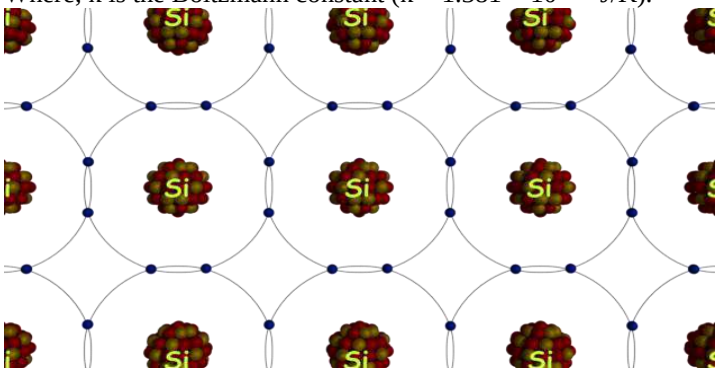
At room temperature resistivity of semiconductor is in between insulators and conductors. Semiconductors show negative temperature coefficient of resistivity that means its resistance decreases with increase in temperature. Both Si and Ge are elements of IV group, i.e. both elements have four valence electrons. Both form the covalent bond with the neighboring atom. At absolute zero temperature both behave like an insulator, i.e. the valence band is full while conduction band is empty but as the temperature is raised more and more covalent bonds break and electrons are set free and jump to the conduction band.

Intrinsic Semiconductors

As per **theory of semiconductor**, semiconductor in its pure form is called as intrinsic semiconductor. In pure semiconductor number of electrons (n) is equal to number of holes (p) and thus conductivity is very low as valence electrons are covalent bonded. In this case we write $n = p = n_i$, where n_i is called the intrinsic concentration. It can be shown that n_i can be written

$$n_i = n_0 T^{\frac{2}{3}} e^{\frac{-V_G}{2V_T}}$$

Where, n_0 is a constant, T is the absolute temperature, V_G is the semiconductor band gap voltage, and V_T is the thermal voltage.
The thermal voltage is related to the temperature by $V_T = kT/q$
Where, k is the Boltzmann constant ($k = 1.381 \times 10^{-23}$ J/K).

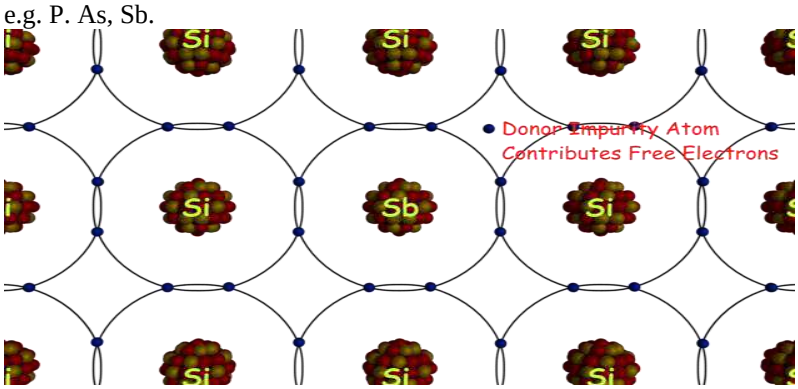


Extrinsic Semiconductors

As per **theory of semiconductor**, impure semiconductors are called extrinsic semiconductors. **Extrinsic semiconductor** is formed by adding a small amount of impurity. Depending on the type of impurity added we have two types of semiconductors: N-type and P-type semiconductors. In 100 million parts of semiconductor one part of impurity is added.

N type Semiconductor

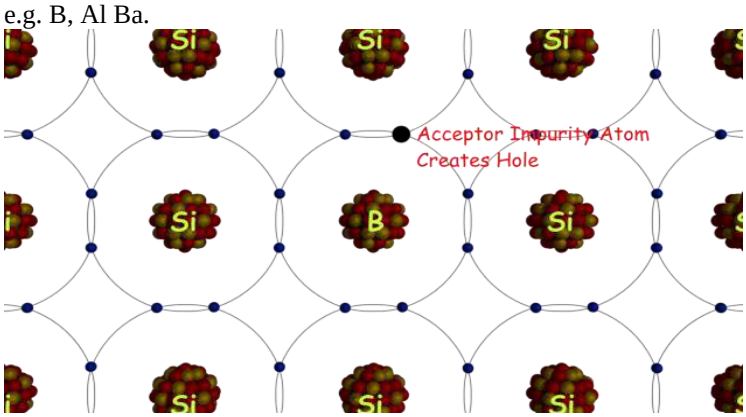
In this type of semiconductor majority carriers are electrons and minority carriers are holes. N – type semiconductor is formed by adding pentavalent (five valence electrons) impurity in pure semiconductor crystal, e.g. P. As, Sb.



Four of the five valence electron of pentavalent impurity forms covalent bond with Si atom and the remaining electron is free to move anywhere within the crystal. Pentavalent impurity donates electron to Si that's why N-type impurity atoms are known as donor atoms. This enhances the conductivity of pure Si. Majority carriers are electrons .

P type Semiconductors

In this type of semiconductor majority carriers are holes, and minority carriers are electrons. The p-type semiconductor is formed by adding trivalent (three valence electrons) impurity in a pure semiconductor crystal, e.g. B, Al Ba.



Three of the four valence electron of tetravalent impurity forms covalent bonds with Si atoms. The phenomenon creates a space which we refer to a hole. When the temperature rises an electron from another covalent bond jumps to fill this space. Hence, a hole gets created behind. In this way conduction takes place. P-type impurity accepts electrons and is called acceptor atom. Majority carriers are holes.

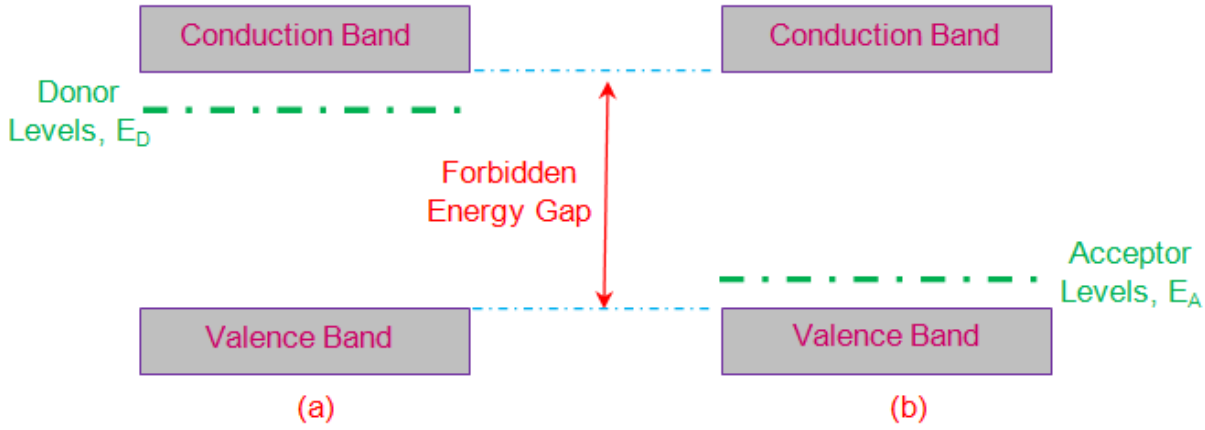


Figure 2 Energy Band Diagram of (a) *n*-type Extrinsic Semiconductor
(b) *p*-type Extrinsic Semiconductor

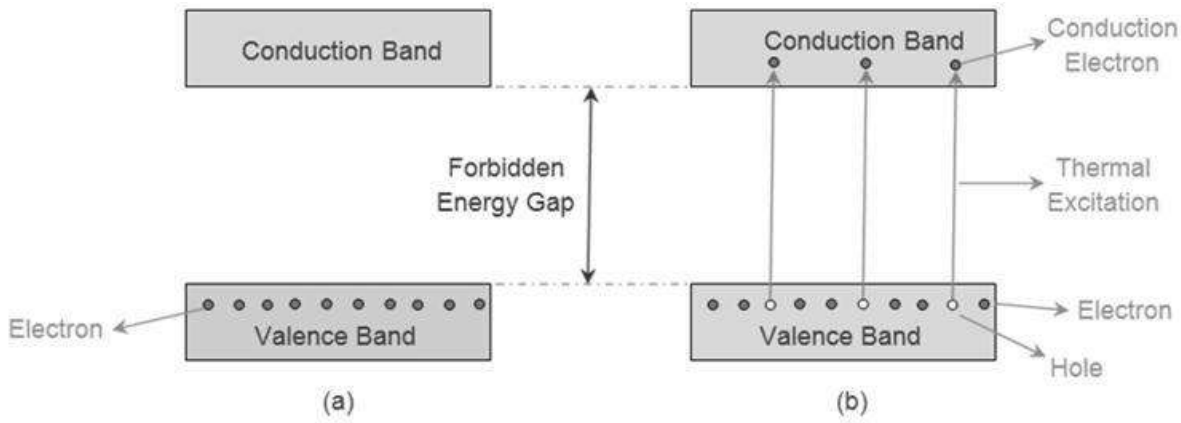


Figure 2 Energy Band Diagram of Intrinsic Semiconductor at (a) 0K (b) Temperature > 0K

SEMICONDUCTOR DIODE

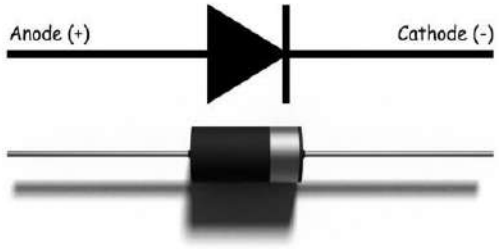
A **diode** is defined as a two-terminal electronic component that only conducts current in one direction (so long as it is operated within a specified voltage level). An ideal diode will have zero resistance in one direction, and infinite resistance in the reverse direction.

Although in the real world, diodes can not achieve zero or infinite resistance. Instead, a diode will have negligible resistance in one direction (to allow current flow), and a very high resistance in the reverse direction (to *prevent* current flow). A diode is effectively like a valve for an electrical circuit.
Semiconductor diodes are the most common type of diode. These diodes begin conducting electricity only if a certain threshold voltage is present in the forward direction (i.e. the "low resistance" direction). The diode is said to be "*forward biased*" when conducting current in this direction. When connected within a circuit in the reverse direction (i.e. the "high resistance" direction), the diode is said to be "*reverse biased*".
A diode only blocks current in the reverse direction (i.e. when it is reverse biased) while the reverse voltage is within a specified range. Above this range, the reverse barrier breaks. The voltage at which this breakdown occurs is called the "reverse breakdown voltage". When the voltage of the circuit is higher than the reverse breakdown voltage, the diode is able to conduct electricity in the reverse direction (i.e. the "high resistance" direction). This is why in practice we say diodes have a high resistance in the reverse direction – not an infinite resistance.

A PN junction is the simplest form of the semiconductor diode. In ideal conditions, this PN junction behaves as a short circuit when it is forward biased, and as an open circuit when it is in the reverse biased. The name diode is derived from "di–ode" which means a device that has two electrodes. Diodes are commonly used in many electronics projects and are included in many of the best Arduino starter kits.

Diode Symbol

The symbol of a diode is shown below. The arrowhead points in the direction of conventional current flow in the forward biased condition. That means the anode is connected to the p side and the cathode is connected to the n side.



We can create a simple PN junction diode by doping pentavalent or donor impurity in one portion and trivalent or acceptor impurity in other portion of silicon or germanium crystal block. These dopings make a PN junction at the middle part of the block. We can also form a PN junction by joining a p-type and n-type semiconductor together with a special fabrication technique. The terminal connected to the p-type is the anode. The terminal connected to the n-type side is the cathode.

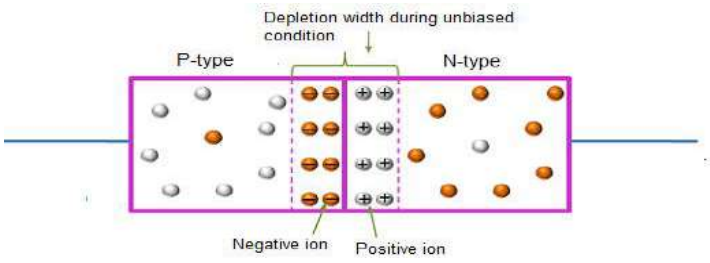
Working Principle of Diode

A diode's working principle depends on the interaction of n-type and p-type semiconductors. An n-type semiconductor has plenty of free electrons and a very few numbers of holes. In other words, we can say that the concentration of free electrons is high and that of holes is very low in an n-type semiconductor. Free electrons in the n-type semiconductor are referred as majority charge carriers, and holes in the n-type semiconductor are referred to as minority charge carriers.
A p-type semiconductor has a high concentration of holes and a low concentration of free electrons. Holes in the p-type semiconductor are majority charge carriers, and free electrons in the p-type semiconductor are minority charge carriers.

Unbiased Diode
Now let us see what happens when one n-type region and one p-type region come in contact. Here due to concentration differences, majority carriers diffuse from one side to another. As the concentration of holes is high in the p-type region and it is low in the n-type region, the holes start diffusing from the p-type region to the n-type region.Again the concentration of free electrons is high in the n-type region and it is low in the p-type region and due to this reason, free electrons start diffusing from the n-type region to the p-type region.

The free electrons diffusing into the p-type region from the n-type region would recombine with holes available there and create uncovered negative ions in the p-type region. In the same way, the holes diffusing into the n-type region from the p-type region would recombine with free electrons available there and create uncovered positive ions in the n-type region.

In this way, there would a layer of negative ions in the p-type side and a layer of positive ions in the n-type region appear along the junction line of these two types of semiconductors. The layers of uncovered positive ions and uncovered negative ions form a region in the middle of the diode where no charge carrier exists since all the charge carriers get recombined here in this region. Due to the lack of charge carriers, this region is called the depletion region.



After the formation of the depletion region, there is no more diffusion of charge carriers from one side to another in the diode. This is due to the electric field appeared across the depletion region will prevent further migration of charge carriers from one side to another.

The potential of the layer of uncovered positive ions in the n-type side would repeal the holes in the p-type side and the potential of the layer of uncovered negative ions in the p-type side would repeal the free electrons in the n-type side. That means a potential barrier is created across the junction to prevent further diffusion of charge carriers.

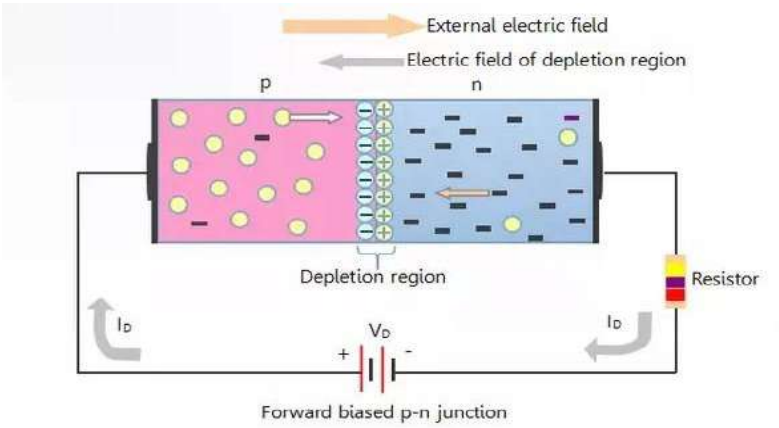
Forward Biased Diode

Now let us see what happens if a positive terminal of a source is connected to the p-type side and the negative terminal of the source is connected to the n-type side of the diode and if we increase the voltage of this source slowly from zero.

In the beginning, there is no current flowing through the diode. This is because although there is an external electrical field applied across the diode, the majority charge carriers still do not get sufficient influence of the external field to cross the depletion region. As we told that the depletion region acts as a potential barrier against the majority charge carriers.

This potential barrier is called forward potential barrier. The majority charge carriers start crossing the forward potential barrier only when the value of externally applied voltage across the junction is more than the potential of the forward barrier. For silicon diodes, the forward barrier potential is 0.7 volt and for germanium diodes, it is 0.3 volt.

When the externally applied forward voltage across the diode becomes more than the forward barrier potential, the free majority charge carriers start crossing the barrier and contribute the forward diode current. In that situation, the diode would behave as a short-circuited path and the forward current gets limited by only externally connected resistors to the diode.



Reverse Biased Diode

Now let us see what happens if we connect the negative terminal of the voltage source to the p-type side and positive terminal of the voltage source to the n-type side of the diode. At that condition, due to electrostatic attraction of the negative potential of the source, the holes in the p-type region would be shifted more away from the junction leaving more uncovered negative ions at the junction.

In the same way, the free electrons in the n-type region would be shifted more away from the junction towards the positive terminal of the voltage source leaving more uncovered positive ions in the junction. As a result of this

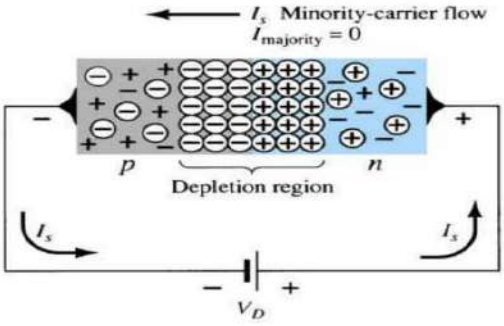
phenomenon, the depletion region becomes wider. This condition of a diode is called the reverse biased condition. At that condition, no majority carriers cross the junction, and they instead move away from the junction. In this way, a diode blocks the flow of current when it is reverse biased.

As we already told at the beginning of this article that there are always some free electrons in the p-type semiconductor and some holes in the n-type semiconductor. These opposite charge carriers in a semiconductor are called minority charge carriers. In the reverse biased condition, the holes find themselves in the n-type side would easily cross the reverse-biased depletion region as the field across the depletion region does not present rather it helps minority charge carriers to cross the depletion region.

As a result, there is a tiny current flowing through the diode from positive to the negative side. The amplitude of this current is very small as the number of minority charge carriers in the diode is very small. This current is called reverse saturation current.

If the reverse voltage across a diode gets increased beyond a safe value, due to higher electrostatic force and due to higher kinetic energy of minority charge carriers colliding with atoms, a number of covalent bonds get broken to contribute a huge number of free electron-hole pairs in the diode and the process is cumulative.

The huge number of such generated charge carriers would contribute a huge reverse current in the diode. If this current is not limited by an external resistance connected to the diode circuit, the diode may permanently be destroyed.



Operation of diode can be summarized in form of I-V **diode characteristics** graph.

For reverse bias diode, $V < 0, I_D = I_S$

Where, V = supply voltage

I_D = diode current

I_S = reverse saturation current

For forward bias, $V > 0,\ I_D = I_S(e^{V/NV_T} - 1)$

Where, V_T = volt's equivalent of temperature = KT/Q = T/11600

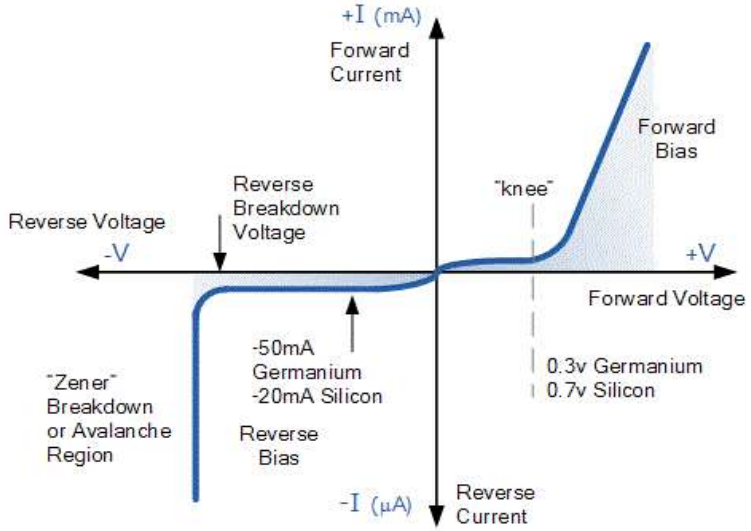
Q = electronic charge = $1.632 \times 10^{-19} C$

K = Boltzmann's constant = 1.38×10^{-23}

N = 1, for Ge

= 2, for Si

V-I CHARACTERSTICS OF DIODE:



As reverse bias voltage is further raised, depletion region width increases and a point comes when junction breaks down. This results in large flow of current. Breakdown is the knee of **diode characteristics** curve. Junction breakdown takes place due to two phenomena.The diode current equation is also known as SHOCKLEY'S EQUATION.

Avalanche Breakdown (for V > 5V)

Under very high reverse bias voltage kinetic energy of minority carriers become so large that they knock out electrons from covalent bonds, which in turn knock more electrons and this cycle continues until and unless junction breakdowns. This is known as avalanche breakdown, a phenomenom that is cental to avalanche diodes.

Zener Effect (for V < 5V)

Under reverse bias voltage junction barrier tends to increase with increase in bias voltage. This results in very high static electric field at the junction. This static electric field breaks covalent bond and set minority carriers free which contributes to reverse current. Current increases abruptly and junction breaks down. This is known as Zener breakdown, and is a phenomenom that is cental to Zener diodes

Static or DC Resistance

It is the resistance offered by the diode to the flow of DC through it when we apply a DC voltage to it. Mathematically the static resistance is expressed as the ratio of DC voltage applied across the diode terminals to the DC flowing through it i.e.

$$R_{dc} = \frac{V_{dc}}{I_{dc}}$$

Dynamic or AC Resistance

It is the resistance offered by the diode to the flow of AC through it when we connect it in a circuit which has an AC voltage source as an active circuit element. Mathematically the dynamic resistance is given as the ratio of change in voltage applied across the diode to the resulting change in the current flowing through it. This is shown by the slope-indicating red solid lines and is expressed as

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

where Δ signifies a finite change in the quantity.

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV}[I_s(e^{kV_D/T_K} - 1)]$$

and

$$\frac{dI_D}{dV_D} = \frac{k}{T_K}(I_D + I_s)$$

following a few basic maneuvers of differential calculus. In general, $I_D \gg I_s$ in the vertical slope section of the characteristics and

$$\frac{dI_D}{dV_D} \cong \frac{k}{T_K} I_D$$

Substituting $\eta = 1$ for Ge and Si in the vertical-rise section of the characteristics, we obtain

$$k = \frac{11{,}600}{\eta} = \frac{11{,}600}{1} = 11{,}600$$

and at room temperature,

$$T_K = T_C + 273° = 25° + 273° = 298°$$

so that

$$\frac{k}{T_K} = \frac{11{,}600}{298} \cong 38.93$$

and

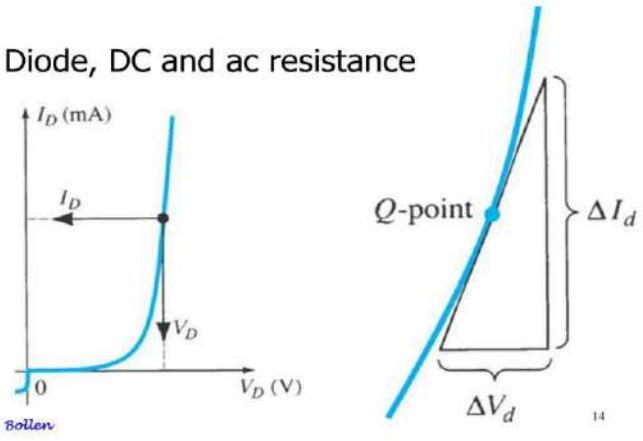
$$\frac{dI_D}{dV_D} = 38.93 I_D$$

Flipping the result to define a resistance ratio ($R = V/I$) gives us

$$\frac{dV_D}{dI_D} \cong \frac{0.026}{I_D}$$

or

$$\boxed{r_d = \frac{26 \text{ mV}}{I_D}} \quad \text{Ge,Si}$$

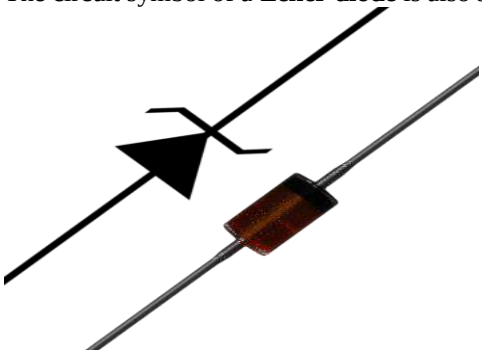


ZENER DIODE

Zener diode is basically like an ordinary PN junction diode but normally operated in reverse biased condition. But ordinary PN junction diode connected in reverse biased condition is not used as Zener diode practically. A Zener diode is a specially designed, highly doped PN junction diode.

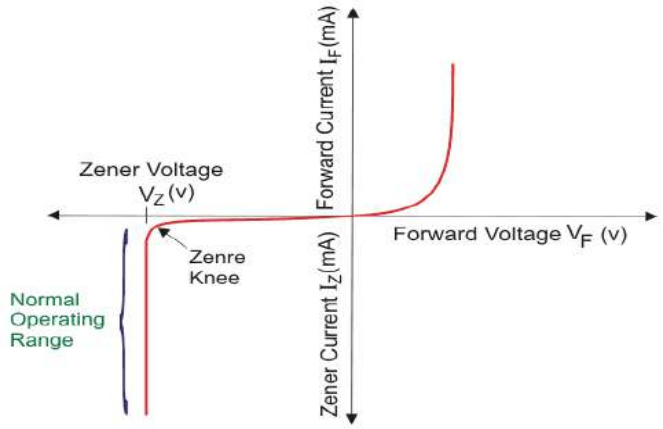
Working Principle of Zener Diode:

When a PN junction diode is reverse biased, the depletion layer becomes wider. If this reverse biased voltage across the diode is increased continually, the depletion layer becomes more and more wider. At the same time, there will be a constant reverse saturation current due to minority carriers.
After certain reverse voltage across the junction, the minority carriers get sufficient kinetic energy due to the strong electric field. Free electrons with sufficient kinetic energy collide with stationary ions of the depletion layer and knock out more free electrons. These newly created free electrons also get sufficient kinetic energy due to the same electric field, and they create more free electrons by collision cumulatively. Due to this commutative phenomenon, very soon, huge free electrons get created in the depletion layer, and the entire diode will become conductive. This type of breakdown of the depletion layer is known as avalanche breakdown, but this breakdown is not quite sharp. There is another type of breakdown in depletion layer which is sharper compared to avalanche breakdown, and this is called Zener breakdown. When a PN junction is diode is highly doped, the concentration of impurity atoms will be high in the crystal. This higher concentration of impurity atoms causes the higher concentration of ions in the depletion layer hence for same applied reverse biased voltage, the width of the depletion layer becomes thinner than that in a normally doped diode.
Due to this thinner depletion layer, voltage gradient or electric field strength across the depletion layer is quite high. If the reverse voltage is continued to increase, after a certain applied voltage, the electrons from the covalent bonds within the depletion region come out and make the depletion region conductive. This breakdown is called Zener breakdown. The voltage at which this breakdown occurs is called Zener voltage. If the applied reverse voltage across the diode is more than Zener voltage, the diode provides a conductive path to the current through it hence, there is no chance of further avalanche breakdown in it. Theoretically, Zener breakdown occurs at a lower voltage level then avalanche breakdown in a diode, especially doped for Zener breakdown. The Zener breakdown is much sharper than avalanche breakdown. The Zener voltage of the diode gets adjusted during manufacturing with the help of required and proper doping. When a **zener diode** is connected across a voltage source, and the source voltage is more than Zener voltage, the voltage across a Zener diode remain fixed irrespective of the source voltage. Although at that condition current through the diode can be of any value depending on the load connected with the diode. That is why we use a Zener diode mainly for controlling voltage in different circuits.
The circuit symbol of a **Zener diode** is also shown below.



Characteristics of a Zener Diode

Now, discussing about the diode circuits we should look through the graphical representation of the operation of the **zener diode**. Normally, it is called the V-I characteristics of a Zener diode.

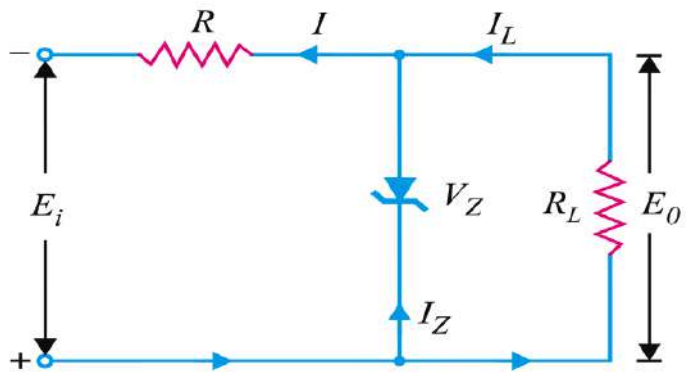


The above diagram shows the V-I characteristics of a zener diode. When the diode is connected in forward bias, this diode acts as a normal diode but when the reverse bias voltage is greater than zener voltage, a sharp breakdown takes place. In the V-I characteristics above V_z is the zener voltage. It is also the knee voltage because at this point the current increases very rapidly.

Operation of Zener Diode Voltage Regulator

A rectifier with an appropriate filter serves as a good source of d.c. output. However, the major disadvantage of such a power supply is that the output voltage changes with the variations in the input voltage or load. Thus, if the input voltage increases, the d.c. output voltage of the rectifier also increases. Similarly, if the load current increases, the output voltage falls due to the voltage drop in the rectifying element, filter chokes, transformer winding etc. In many electronic applications, it is desired that the output voltage should remain constant regardless of the variations in the input voltage or load. In order to ensure this, a voltage stabilising device, called voltage stabiliser is used. Several stabilising circuits have been designed but only *zener diode* as a voltage stabiliser.
A zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range. The circuit arrangement is shown in Fig (*i*). The zener diode of zener voltage *Vz* is reverse connected across the load *RL* across which constant output is desired. The series resistance *R* absorbs the output voltage fluctuations so as to maintain constant voltage across the load. It may be noted that the zener will maintain a constant voltage *Vz* (= *E*0) across the load so long as the input voltage does not fall below *Vz*

fig (i)



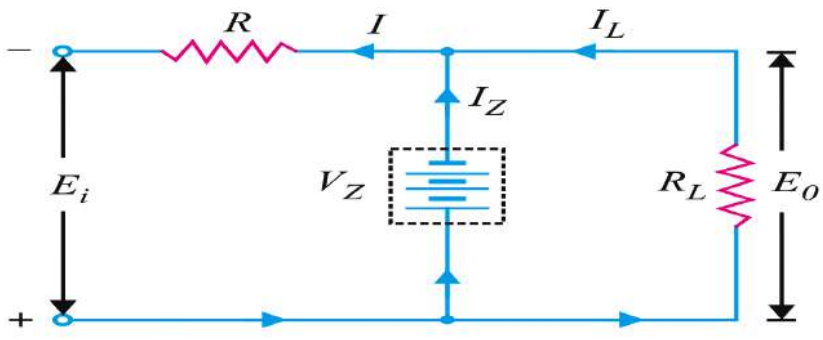
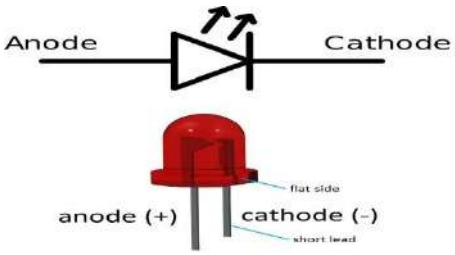


Fig- (ii)

When the circuit is properly designed, the load voltage *E*0 remains essentially constant (equal to *Vz*) even though the input voltage *Ei* and load resistance *RL* may vary over a wide range.
(*i*) Suppose the input voltage increases. Since the zener is in the breakdown region, the zener diode is equivalent to a battery *VZ* as shown in Fig (*ii*). It is clear that output voltage remains constant at *VZ* (= *E*0). The excess voltage is dropped across the series resistance *R*. This will cause an increase in the value of total current *I*. The zener will conduct the increase of current in *I* while the load current remains constant. Hence, output voltage *E*0 remains constant irrespective of the changes in the input voltage *Ei*.
(*ii*) Now suppose that input voltage is constant but the load resistance *RL* decreases. This will cause an increase in load current. The extra current cannot come from the source because drop in *R* (and hence source current *I*) will not change as the zener is within its regulating range. The additional load current will come from a decrease in zener current *IZ*. Consequently, the output voltage stays at constant value.
Voltage drop across $R = Ei - E0$
Current through *R*, $I = IZ + IL$
Applying Ohm's law, we have

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

Light Emitting Diode (**LED**):



A **Light Emitting Diode** (**LED**) is a special type of PN junction diode. The light emitting diode is specially doped and made of a special type of semiconductor. This diode can emit light when it is in the forward biased state. Aluminum indium gallium phosphide (AlInGaP) and indium gallium nitride (InGaN) are two of the most commonly used semiconductors for LED technologies.

Older LED technologies used gallium arsenide phosphide (GaAsP), gallium phosphide (GaP), and aluminum gallium arsenide (AlGaAs). LEDs generate visible radiation by electroluminescence phenomenon when a low-voltage direct current is applied to a suitably doped crystal containing a p-n junction, as shown in the diagram.

The doping is typically carried out with elements from column III and V of the periodic table. When a forward biased current, I_F, energizes the p-n junction, it emits light at a wavelength defined by the active region energy gap, E_g.
When the forward biased current I_F is applied through the p-n junction of the diode, minority carrier electrons are injected into the p-region and corresponding minority carrier electrons are injected into the n-region. Photon emission occurs due to electron-hole recombination in the p-region.

Color of an LED
The color of an LED device is expressed in terms of the dominant wavelength emitted, λd (in nm). AlInGaP LEDs produce the colors red (626 to 630 nm), red-orange (615 to 621 nm), orange (605 nm), and amber (590 to 592 nm). InGaN LEDs produce the colors green (525 nm), blue green (498 to 505 nm), and blue (470 nm). The color and forward voltage of AlInGaP LEDs depend on the temperature of the LED p-n junction.
"Liquid Crystal Display"- LCD:

Stands for "Liquid Crystal Display." LCD is a flat panel display technology commonly used in TVs and computer monitors. It is also used in screens for mobile devices, such as laptops, tablets, and smartphones.

LCD displays don't just look different than bulky CRT monitors, the way they operate is significantly different as well. Instead of firing electrons at a glass screen, an LCD has backlight that provides light to individual pixels arranged in a rectangular grid. Each pixel has a red, green, and blue RGB sub-pixel that can be turned on or off. When all of a pixel's sub-pixels are turned off, it appears black. When all the sub-pixels are turned on 100%, it appears white. By adjusting the individual levels of red, green, and blue light, millions of color combinations are possible.

How an LCD works

The backlight in liquid crystal display provides an even light source behind the screen. This light is polarized, meaning only half of the light shines through to the liquid crystal layer. The liquid crystals are made up of a part solid, part liquid substance that can be "twisted" by applying electrical voltage to them. They block the polarized light when they are off, but reflect red, green, or blue light when activated.

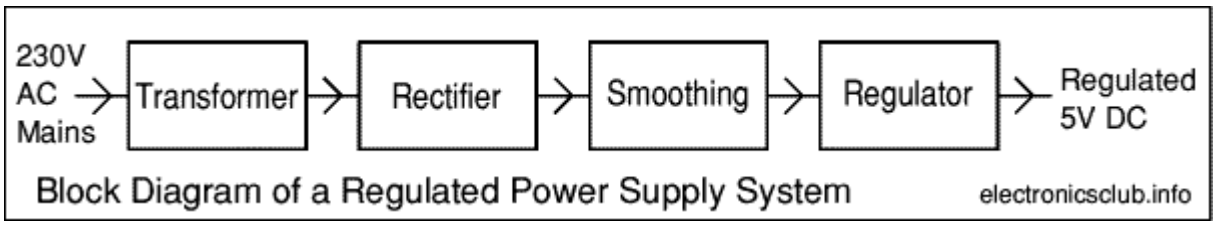
Each LCD screen contains a matrix of pixels that display the image on the screen. Early LCDs had passive-matrix screens, which controlled individual pixels by sending a charge to their row and column. Since a limited number of electrical charges could be sent each second, passive-matrix screens were known for appearing blurry when images moved quickly on the screen. Modern LCDs typically use active-matrix technology, which contain thin film transistors, or TFTs. These transistors include capacitors that enable individual pixels to "actively" retain their charge. Therefore, active-matrix LCDs are more efficient and appear more responsive than passive-matrix displays.
NOTE: An LCD's backlight may either be a traditional bulb or LED light. An "LED display" is simply an LCD screen with an LED backlight. This is different than an OLED display, which lights up individual LEDs for each pixel. While the liquid crystals block most of an LCD's backlight when they are off, some of the light may still shine through (which might be noticeable in a dark room). Therefore OLEDs typically have darker black levels than LCDs.

RECTIFIER

DC Power Supply

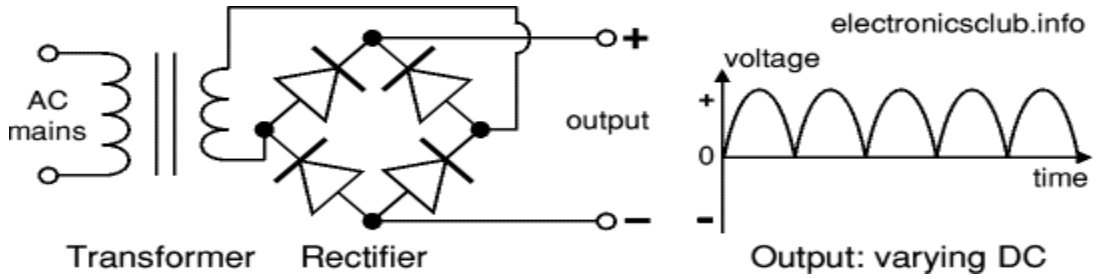
There are many types of power supply. Most are designed to convert high voltage AC mains electricity to a suitable low voltage supply for electronics circuits and other devices. A power supply can by broken down into a series of blocks, each of which performs a particular function.

For example a 5V regulated supply:



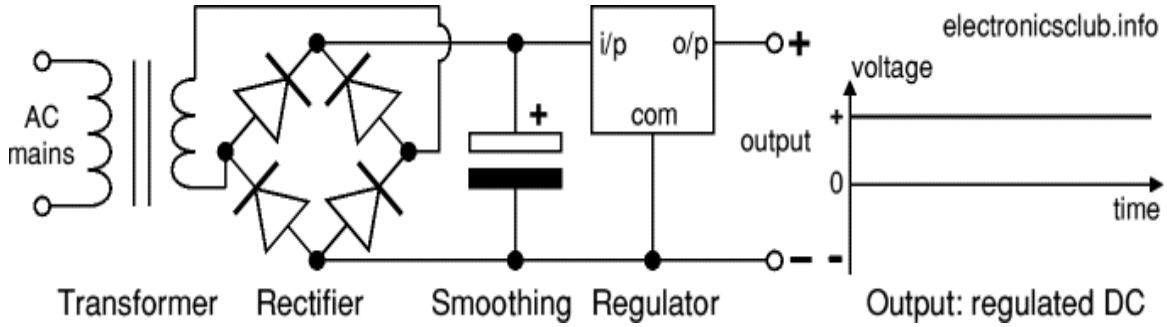
- Transformer - steps down high voltage AC mains to low voltage AC.
- Rectifier - converts AC to DC, but the DC output is varying.
- Smoothing - smooths the DC from varying greatly to a small ripple.
- Regulator - eliminates ripple by setting DC output to a fixed voltage.

Transformer + Rectifier



The **varying DC** output is suitable for lamps, heaters and standard motors. It is **not** suitable for electronic circuits unless they include a smoothing capacitor.

Transformer + Rectifier + Smoothing + Regulator

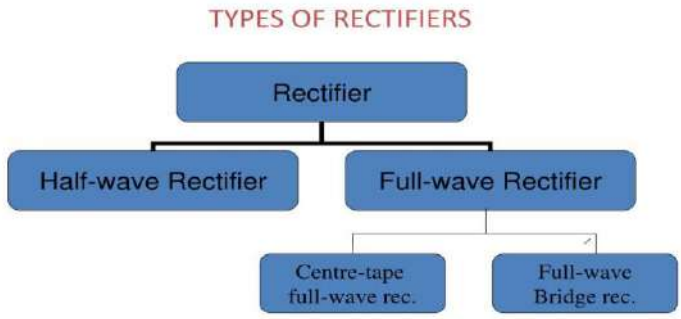


The **regulated DC** output is very smooth with no ripple. It is suitable for all electronic circuits.

RECTIFIER

In a large number of electronic circuits, we require DC voltage for operation. We can easily convert the AC voltage or AC current into DC voltage or DC current by using a device called P-N junction diode.

One of the most important applications of a P-N junction diode is the rectification of Alternating Current (AC) into Direct Current (DC). A P-N junction diode allows electric current in only forward bias condition and blocks electric current in reverse bias condition. In simple words, a diode allows electric current in one direction. This unique property of the diode allows it to acts like a rectifier.



HALF WAVE RECTIFIER

A **half wave rectifier** is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. Half-wave rectifiers are used to convert AC voltage to DC voltage, and only require a single diode to construct.

A rectifier is a device that converts alternating current (AC) to direct current (DC). It is done by using a diode or a group of diodes. Half wave rectifiers use one diode, while a full wave rectifier uses multiple diodes.
The working of a half wave rectifier takes advantage of the fact that diodes only allow current to flow in one direction.

Half Wave Rectifier Theory

A half wave rectifier is the simplest form of rectifier available. The diagram below illustrates the basic principle of a half-wave rectifier. When a standard AC waveform is passed through a half-wave rectifier, only half of the AC waveform remains. Half-wave rectifiers only allow one half-cycle (positive or negative half-cycle) of the AC voltage through and will block the other half-cycle on the DC side, as seen below.

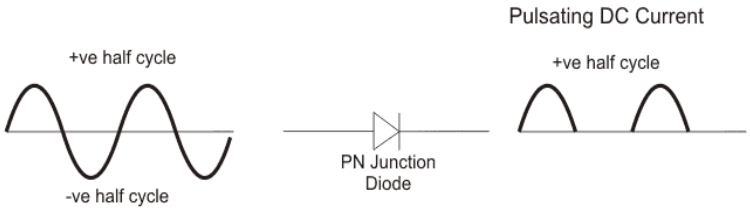


Figure - 1

Only one diode is required to construct a half-wave rectifier. In essence, this is all that the half-wave rectifier is doing.Since DC systems are designed to have current flowing in a single direction, putting an AC waveform with positive and negative cycles through a DC device can have destructive (and dangerous) consequences. So we use half-wave rectifiers to convert the AC input power into DC output power.

But the diode is only part of it – a complete half-wave rectifier circuit consists of 3 main parts:

1. A transformer
2. A resistive load
3. A diode

A half wave rectifier circuit diagram looks like this:

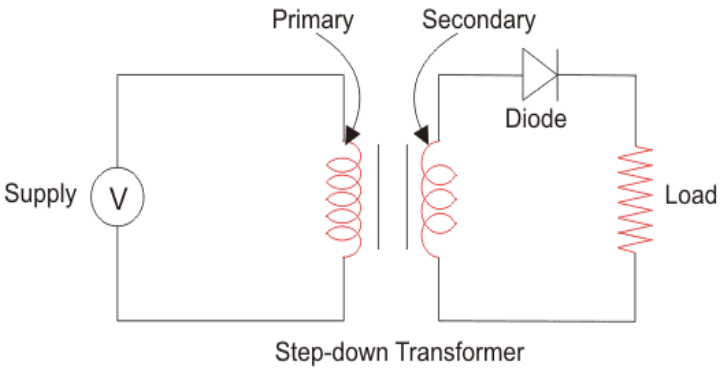


Figure - 2

We'll now go through the process of how a half-wave rectifier converts an AC voltage to a DC output.

First, a high AC voltage is applied to the to the primary side of the step-down transformer and we will get a low voltage at the secondary winding which will be applied to the diode.

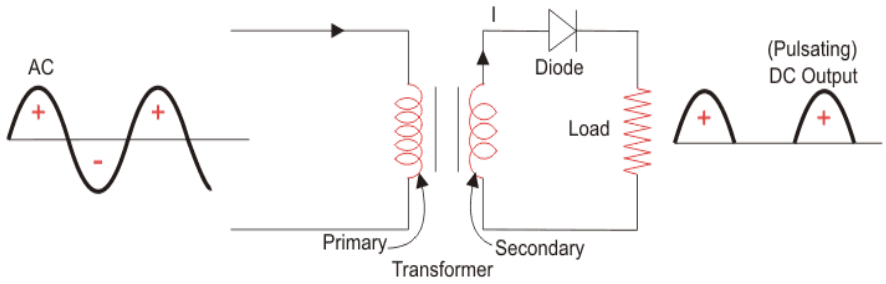
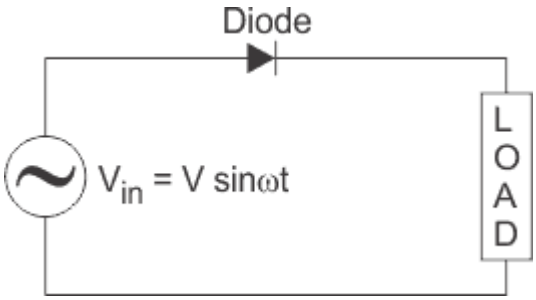


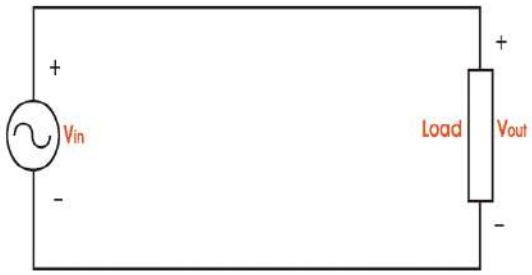
Figure - 3

During the positive half cycle of the AC voltage, the diode will be forward biased and the current flows through the diode. During the negative half cycle of the AC voltage, the diode will be reverse biased and the flow of current will be blocked. The final output voltage waveform on the secondary side (DC) is shown in figure 3 above.

If we replace the secondary transformer coils with a source voltage, we can simplify the circuit diagram of the half-wave rectifier as:

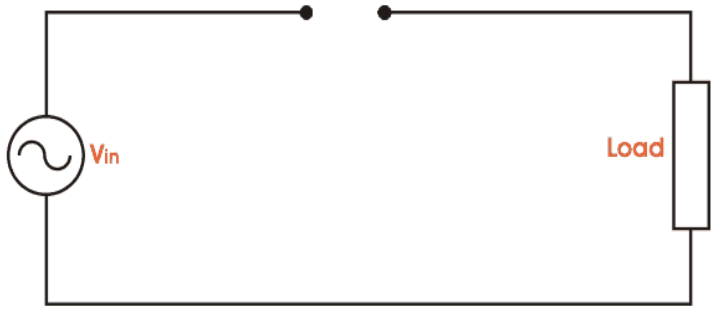


For the positive half cycle of the AC source voltage, the equivalent circuit effectively becomes:



This is because the diode is forward biased, and is hence allowing current to pass through. So we have a closed circuit.

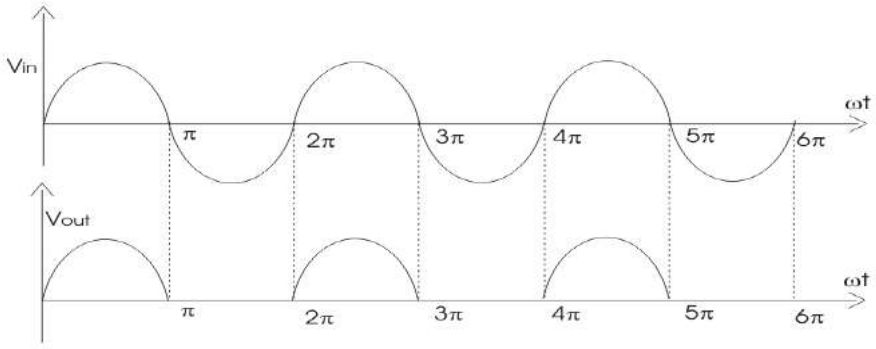
But for the negative half cycle of the AC source voltage, the equivalent circuit becomes:



Because the diode is now in reverse bias mode, no current is able to pass through it. As such, we now have an open circuit. Since current can not flow through to the load during this time, the output voltage is equal to zero.

This all happens very quickly – since an AC waveform will oscillate between positive and negative many times each second (depending on the frequency).

Here's what the half wave rectifier waveform looks like on the input side (V_{in}), and what it looks like on the output side (V_{out}) after rectification (i.e. conversion from AC to DC):



The graph above actually shows a positive half wave rectifier. This is a half-wave rectifier which only allows the positive half-cycles through the diode, and blocks the negative half-cycle.

The voltage waveform before and after a positive half wave rectifier is shown in figure 4 below.

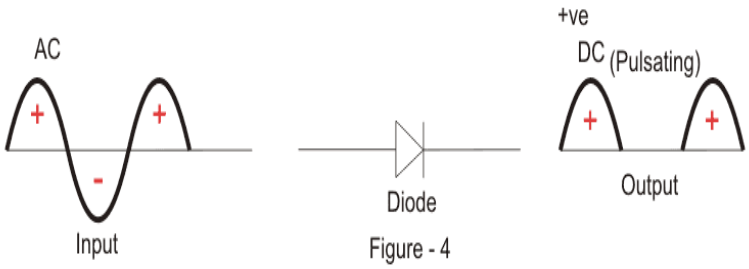


Figure - 4

Conversely, a negative half-wave rectifier will only allow negative half-cycles through the diode and will block the positive half-cycle. The only difference between a positive and negative half wave rectifier is the direction of current or voltage of the diode.As you can see in figure 5 below, the diode is now in the opposite direction. Hence the diode will now be forward biased only when the AC waveform is in its negative half cycle.

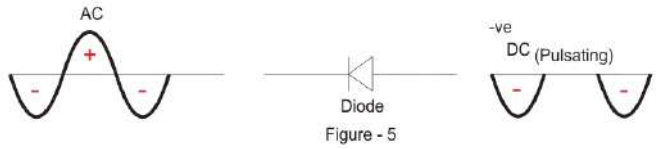


Figure - 5

Output frequency of rectifier is always equal to input frequency.

d.c. power. The output current is pulsating direct current. Therefore, in order to find d.c. power, average current has to be found out.

$$*I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\, d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L}\, d\theta$$

$$= \frac{V_m}{2\pi(r_f + R_L)}\int_0^{\pi} \sin\theta\, d\theta = \frac{V_m}{2\pi(r_f + R_L)}[-\cos\theta]_0^{\pi}$$

$$= \frac{V_m}{2\pi(r_f + R_L)} \times 2 = \frac{V_m}{(r_f + R_L)} \times \frac{1}{\pi}$$

$$= {}^{**}\frac{I_m}{\pi} \qquad \left[\because I_m = \frac{V_m}{(r_f + R_L)}\right]$$

$$\therefore \quad \text{d.c. power, } P_{dc} = I_{dc}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L \qquad \ldots(i)$$

a.c. power input : The a.c. power input is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a half-wave rectified wave, $I_{rms} = I_m/2$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{2}\right)^2 \times (r_f + R_L) \qquad \ldots(ii)$$

$$\therefore \quad \text{Rectifier efficiency} = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 (r_f + R_L)}$$

$$= \frac{0.406\, R_L}{r_f + R_L} = \frac{0.406}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Max. rectifier efficiency = 40.6%

This shows that in half-wave rectification, a maximum of 40.6% of a.c. power is converted into d.c. power.

* Average value $= \dfrac{\text{Area under the curve over a cycle}}{\text{Base}} = \dfrac{\int_0^{\pi} i\, d\theta}{2\pi}$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_m^2 \sin^2 \omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \, d(\omega t)\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[\int_0^{\pi} \frac{1-\cos 2wt}{2} \, d(\omega t)\right]}$$

$$\therefore \; I_{rms} = \frac{I_m}{2}$$

Peak Inverse Voltage (PIV) is the maximum voltage that the diode can withstand during reverse bias condition. If a voltage is applied more than the PIV, the diode will be destroyed.

Disadvantages : The main disadvantages of a half-wave rectifier are :

(*i*) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

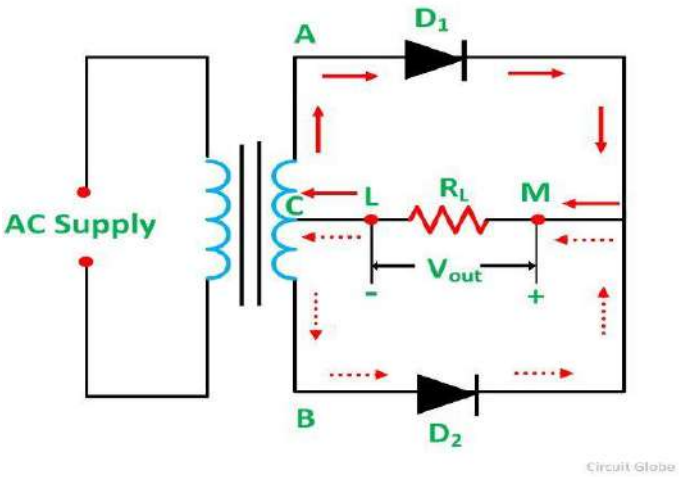
(*ii*) The a.c. supply delivers power only half the time. Therefore, the output is low.

FULL WAVE RECTIFIERS

If rectifiers rectify both the positive and negative half cycles of an input alternating waveform, the rectifiers are referred as full wave rectifiers. Alternatively, we can say, a rectifier is a device that converts alternating current (AC) to direct current (DC). It does it by using a diode or a group of diodes.

CENTER TAPPED FULL WAVE RECTIFIER

The **Center Tapped Full Wave Rectifier** employs a transformer with the secondary winding AB tapped at the centre point C. It converts the AC input voltage into DC voltage The two diode D_1, and D_2 are connected in the circuit as shown in the circuit diagram below.



Each diode uses one-half cycle of the input AC voltage. The diode D_1 utilises the AC voltage appearing across the upper half (AC) of the secondary winding for rectification. The diode D_2 uses the lower half (CB) of the secondary winding.

Operation of the Center Tapped Full Wave Rectifier

When AC supply is switched ON the alternating voltage, V_{in} appears across the terminals AB of the secondary winding of the STEPDOWN transformer. During the positive half cycle of the secondary voltage, the end A becomes positive, and end B becomes negative. Thus, the diode **D_1** becomes **forward biased**, and diode **D_2** becomes **reversed biased.STEPDOWN TRANSFORMER is used to convert high value of AC voltage to lower AC values.**The two diodes conduct simultaneously. Therefore, when the diode D_1 conducts, the diode D_2 does not conduct and vice versa.

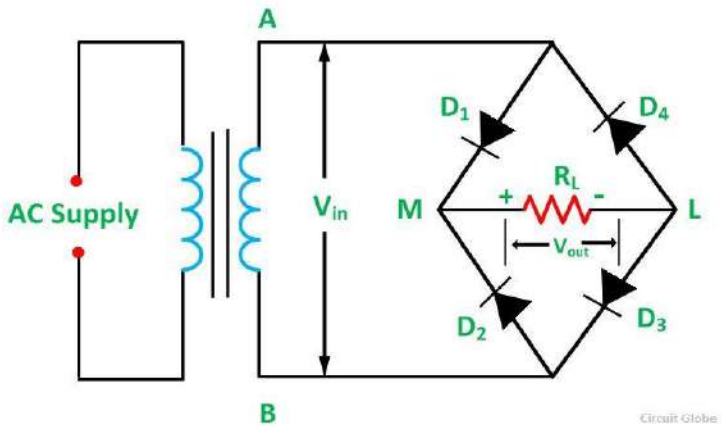
When the Diode D_1 is conducting, the current (i) flows through the diode D_1 load resistor R_L (from M to L) and the upper half of the secondary winding as shown in the circuit diagram marked by the red colour arrow heads. During the negative half cycle, the end B becomes positive and end A becomes negative. This makes the diode D_2 forward biased, and diode D_1 reverse biased.

When the diode D_2 conducts while the diode D_1 does not. The current (i) flows through the diode D_2 load resistor R_L (from M to L) and the lower half of the secondary winding as shown by the red dotted arrows.

The current flowing through the load resistor R_L is in the same direction (i.e., from M to L) during both the positive as well as the negative half cycle of the input. Hence, the DC output voltage ($V_{out} = i\ R_L$) is obtained across the load resistor.

FULL WAVE BRIDGE RECTIFIER

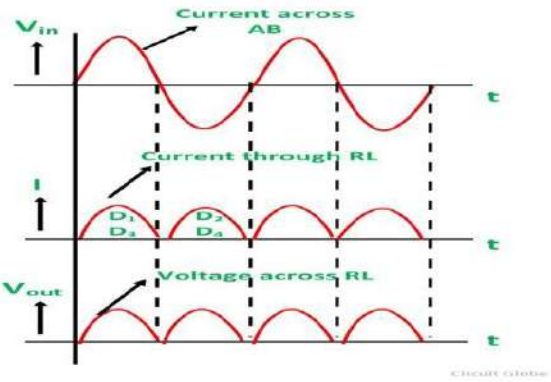
In **Full Wave Bridge Rectifier**, an ordinary transformer is used in place of a center tapped transformer. The circuit forms a bridge connecting the four diodes D_1, D_2, D_3, and D_4. The circuit diagram of Full Wave Bridge Rectifier is shown below. **STEPDOWN TRANSFORMER is used to convert high value of AC voltage to lower AC values.**



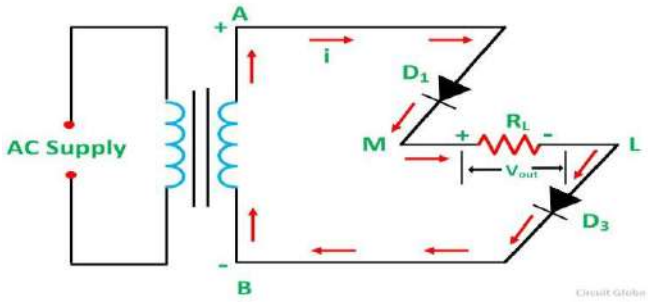
The AC supply which is to be rectified is applied diagonally to the opposite ends of the bridge. Whereas, the load resistor R_L is connected across the remaining two diagonals of the opposite ends of the bridge.

Operation of Full Wave Bridge Rectifier

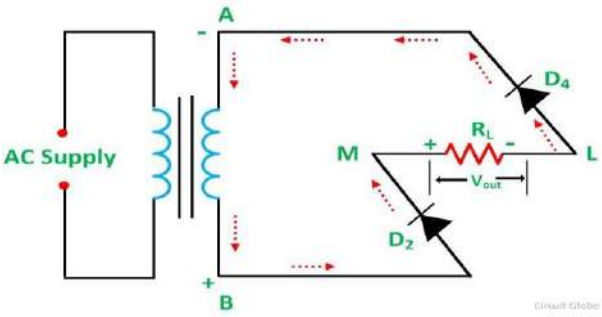
When an AC supply is switched ON, the alternating voltage V_{in} appears across the terminals AB of the secondary winding of the transformer which needs rectification. During the positive half cycle of the secondary voltage, the end A becomes positive, and end B becomes negative as shown in the figure below.



The diodes D_1 and D_3 are forward biased and the diodes D_2 and D_4 is reversed biased. Therefore, diode D_1 and D_3 conduct and diode D_2 and D_4 does not conduct. The current (i) flows through diode D_1, load resistor R_L (from M to L), diode D_3 and the transformer secondary. The waveform of the full wave bridge rectifier is shown above.



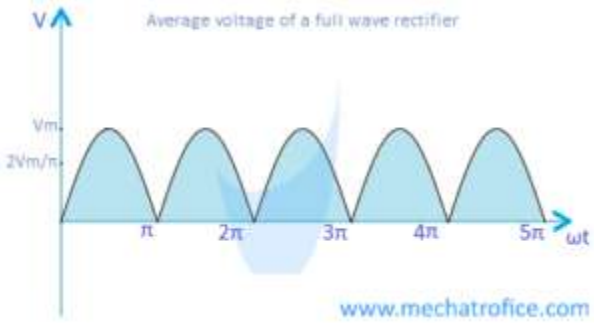
During the negative half cycle, the end A becomes negative and end B positive as shown in the figure below.



From the above diagram, it is seen that the diode D_2 and D_4 are under forward bias and the diodes D_1 and D_3 are reverse bias. Therefore, diode D_2 and D_4 conduct while diodes D_1 and D_3 does not conduct. Thus, current (i) flows through the diode D_2, load resistor R_L (from M to L), diode D_4 and the transformer secondary.

The current flows through the load resistor R_L in the same direction (M to L) during both the half cycles. Hence, a DC output voltage V_{out} is obtained across the load resistor.

Average value of Full wave rectifier



In a full wave rectifier, the negative polarity of the wave will be converted to positive polarity. So the average value can be found by taking the average of one positive half cycle.

Derivation for average current of a full wave rectifier,

$$\frac{1}{2\pi}\int_0^{2\pi} id\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta d\theta$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637 I_m .$$

$$\boxed{I_{dc} = 0.637 I_m.}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

Average voltage equation for a full wave rectifier is $V_{DC} = 2V_m/\pi$.
So during calculations, the average voltage can be obtained by substituting the value of maximum voltage in the equation for V_{DC}.

RMS value of current for full wave rectifier:

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2\, d(wt)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2 wt\, d(wt)}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi} \frac{(1-\cos 2wt)}{2} d(wt)}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{\pi}\left|\frac{wt}{2} - \frac{\sin 2wt}{wt}\right|_0^{\pi}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_{dc} = \frac{2I_m}{\pi}$$

$$\therefore \quad \text{d.c. power output, } P_{dc} = I_{dc}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

a.c. input power. The a.c. input power is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a full-wave rectified wave, we have,

$$I_{rms} = I_m/\sqrt{2}$$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$

$\therefore$ Full-wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)} = \frac{0.812\, R_L}{r_f + R_L} = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Maximum efficiency = 81.2%

Advantages of Full Wave Rectifiers

- Full wave rectifiers have higher rectifying efficiency than half-wave rectifiers. This means that they convert AC to DC more efficiently.
- They have low power loss because no voltage signal is wasted in the rectification process.
- The output voltage of centre-tapped full wave rectifier has lower ripples than a halfwave rectifiers.

Disadvantages of Full Wave Rectifiers

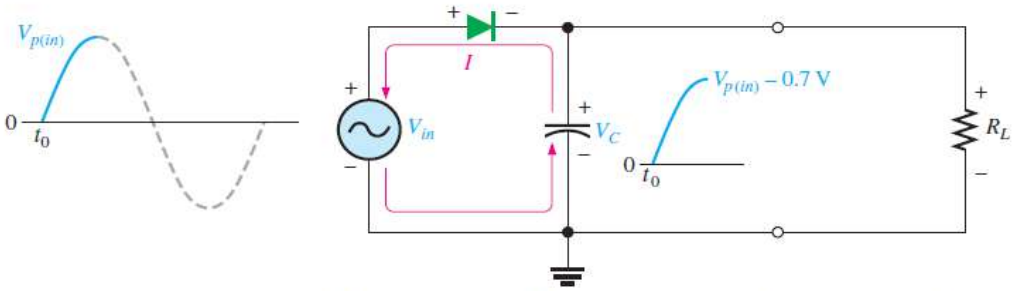
- The centre-tapped rectifier is more expensive than half-wave rectifier and tends to occupy a lot of space.

CAPACITOR-INPUT FILTER

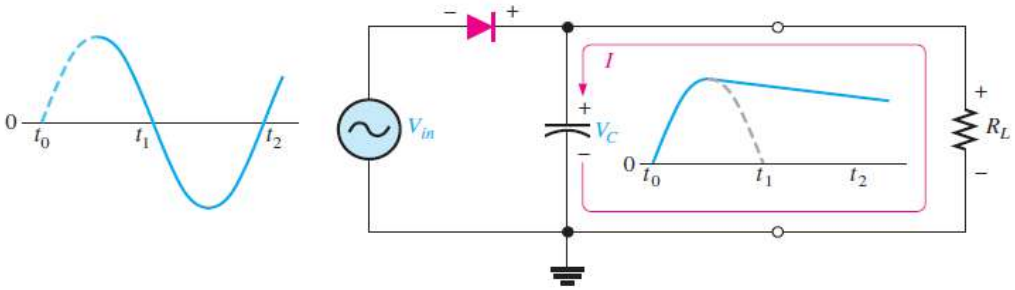
A half-wave rectifier with a capacitor-input filter is shown in Figure below. The filter is simply a capacitor connected from the rectifier output to ground. RL represents the equivalent resistance of a load. We will use the half-wave rectifier to illustrate the basic principle and then expand the concept to full-wave rectification.Both capacitor and load resistor are parallel. During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7 V of the input peak, as illustrated in Figure (a).

When the input begins to decrease below its peak, as shown in part (b), the capacitor retains its charge and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only

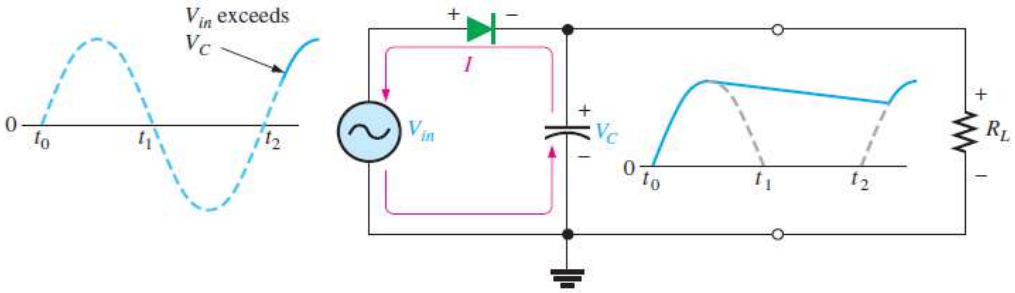
through the load resistance at a rate determined by the RLC time constant, which is normally long compared to the period of the input. The larger the time constant, the less the capacitor will discharge. During the first quarter of the next cycle, as illustrated in part (c), the diode will again become forward-biased when the input voltage exceeds the capacitor voltage by approximately 0.7 V(Si)



(a) Initial charging of the capacitor (diode is forward-biased) happens only once when power is turned on.



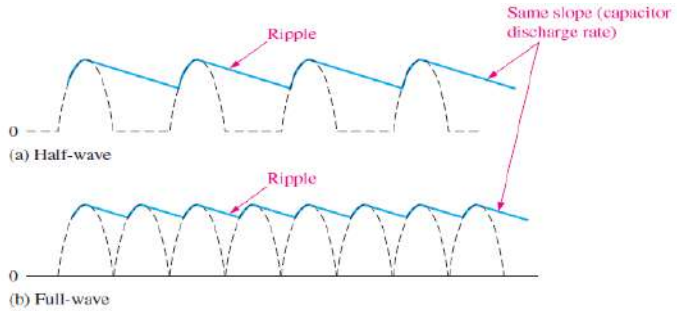
(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid dark blue curve.



(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid dark blue curve.

Ripple Factor of Half Wave Rectifier

'Ripple' is the unwanted AC component remaining when converting the AC voltage waveform into a DC waveform. Even though we try out best to remove all AC components, there is still some small amount left on the output side which pulsates the DC waveform. This undesirable AC component is called 'ripple'.



To quantify how well the half-wave rectifier can convert the AC voltage into DC voltage, we use what is known as the ripple factor (represented by γ or r). The ripple factor is the ratio between the RMS value of the AC voltage (on the input side) and the DC voltage (on the output side) of the rectifier.
The formula for ripple factor is:

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

Which can also be rearranged to equal:

$$Ripple\ factor(r) = \frac{(I_{rms}^2 - I_{dc}^2)}{I_{dc}} = 1.21$$

The ripple factor of half wave rectifier is equal to 1.21 (i.e. γ = 1.21).

Note that for us to construct a good rectifier, we want to keep the ripple factor as low as possible. This is why we use capacitors and inductors as filters to reduce the ripples in the circuit.

Ripple voltage for HWR:
$V_r = V_{peak}$(rectified at the output)/RfC

Filter Circuit for centre tapped FWR:

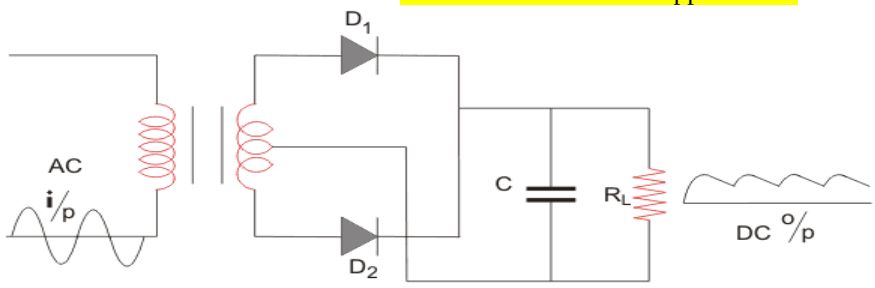


Figure - 9

Filter Circuit for bridge FWR

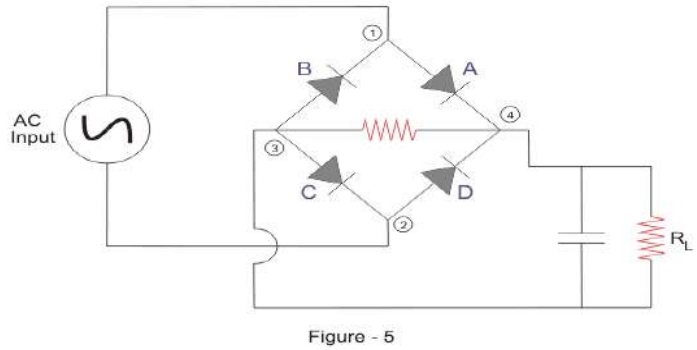


Figure - 5

Ripple Factor (γ)

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

The output we will get from the rectifier will consist of both AC and DC components. The AC components are undesirable to us and will cause pulsations in the output. This unwanted AC components are called Ripple. The expression ripple factor is given above where V_{rms} is the RMS value of the AC component and V_{dc} is the DC component in the rectifier.
For centre-tapped full-wave rectifier, we obtain $\gamma = 0.48$
Note: For us to construct a good rectifier, we need to keep the ripple factor as minimum as possible. We can use capacitors or inductors to reduce the ripples in the circuit.

RIPPLE VOLTAGE FOR FWR:

$V_r = V_{peak}$(rectified at the output)/2RfC

S. No.	Particulars	Half-wave	Centre-tap	Bridge type
1	No. of diodes	1	2	4
2	Transformer necessary	no	yes	no
3	Max. efficiency	40.6%	81.2%	81.2%
4	Ripple factor	1.21	0.48	0.48
5	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
6	Peak inverse voltage	V_m	$2V_m$	V_m

★ ★ ★ ★ ★ ★ ★

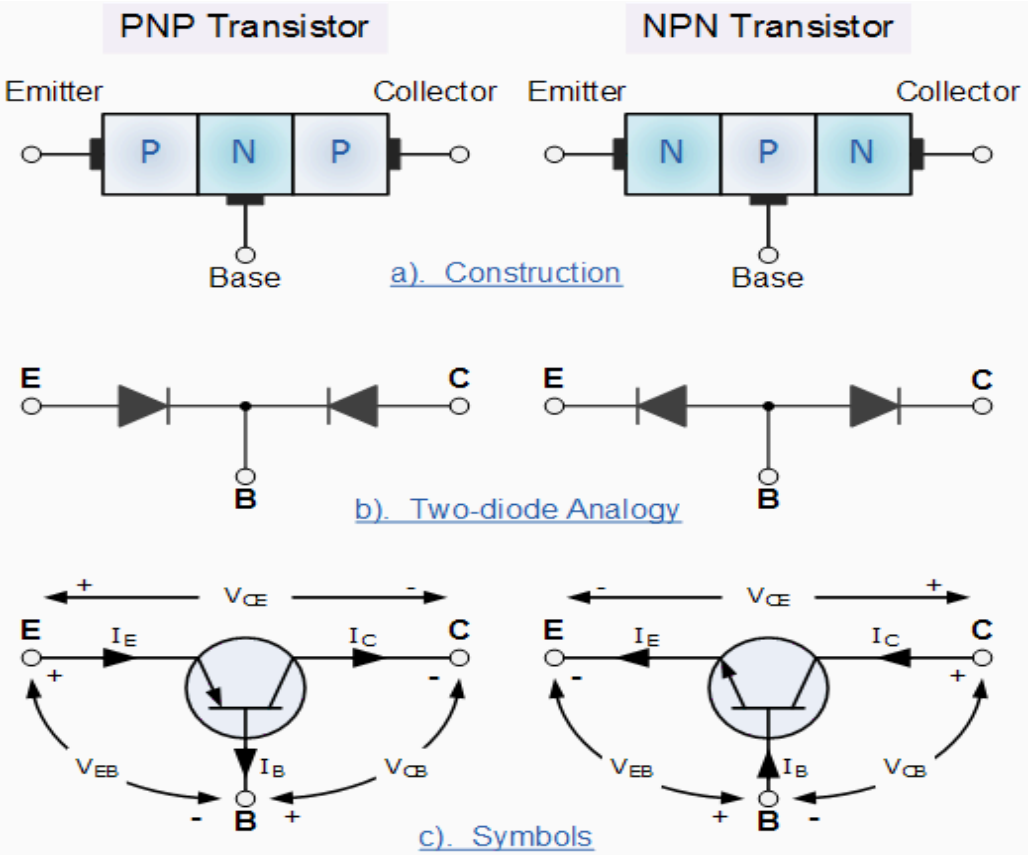
MODULE-II
BIPOLAR JUNCTION TRANSISTOR

W. Shockley, J. Barden and W. Bratterin invented the transistor in 1947. The term 'transistor' is derived from the words 'transfer' and 'resistor.' These words describe the operation of a BJT which is the transfer of an input signal from a low resistance circuit to a high resistance circuit. The abbreviation BJT, from bipolar junction transistor, is often applied to this three terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device.

What is a Bipolar Junction Transistor (BJT)?

A bipolar junction transistor is a three-terminal semiconductor device that consists of two p-n junctions which are able to amplify or magnify a signal. It is a current controlled device. The three terminals of the BJT are the base, the collector and the emitter. A signal of small amplitude applied to the base is available in the amplified form at the collector of the transistor. This is the amplification provided by the BJT. Note that it does require an external source of DC power supply to carry out the amplification process. Bipolar transistors are manufactured in two types, **PNP** and **NPN**, and are available as separate components, usually in large quantities. The prime use or function of this type of transistor is to amplify current. This makes them useful as switches or amplifiers. They have a wide application in electronic devices like mobile phones, televisions, radio transmitters and industrial control.

Bipolar Transistor Construction



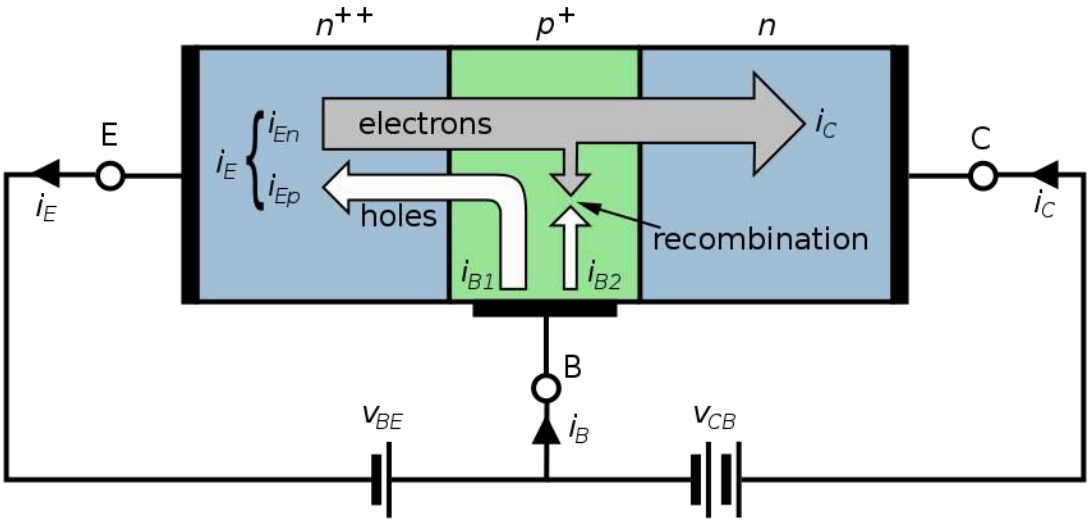
According to dopping:

E>C>B

According to Width:

C>E>B

ACTION OF TRANSISTOR



- Two batteries are used to simplify operation theory. Most applications require one voltage source. The negative terminal of the battery is connected to the N emitter.
- The positive terminal of the same battery is connected to the P-type base. Therefore, the emitter-base circuit is forward biased.
- In the collector circuit, the N collector is connected to the positive battery terminal. The P base is connected to the negative terminal.
- The collector-base circuit is reverse biased.
- Electrons enter the emitter from the negative battery source and flow toward the junction. The forward bias has reduced the potential barrier of the first junction.
- The electrons then combine with the hole carriers in the base to complete the emitter-base circuit. However, the base is a very thin section, about 0.001 inches.
- Most of the electrons flow on through to the collector as the collector terminal is connected to positive terminal of battery and this reverse biased potential is very large so most of the majority charge carriers are attracted and will cross the large base to collector depletion region due to large reverse biased potential.
- there will be an injection of minority carriers(holes) from N dopped collector into the P-type base region material as the collector terminal is connected to positive terminal of battery.Similarly minority charge carriers(free electrons) in the base will move towards collector.Due to this a current will flow from collector terminal towards base due to the presence of minority charge carriers.So total collector current will be:

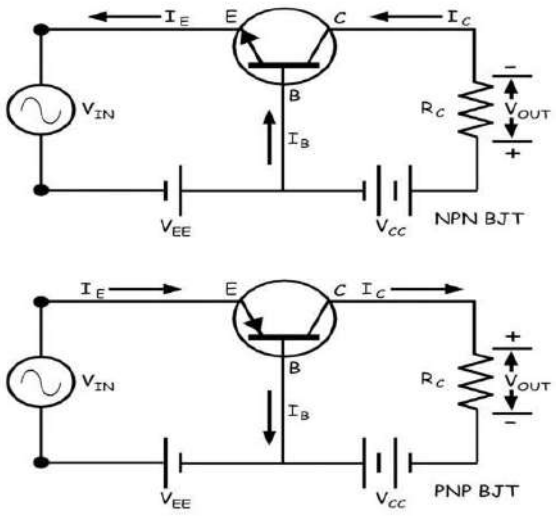
$I_C = I_C$ majority + I_{CO} minority

- The minority-current component is called as:
- leakage current and is given the symbol I_{CO} (I_C current with emitter terminal Open).
- Approximately 95 to 98 percent of the current through the transistor is from an emitter to collector. About two to five percent of the current moves between emitter and base.
- A small change in emitter to base bias voltage causes a somewhat larger change in emitter-collector current. This is what allows transistors to be used as amplifiers. The emitter-base current change, however, is quite small.

$$I_E = I_C + I_B$$

Junction type	Applied voltages	Junction bias		Mode
		B-E	B-C	
NPN	E < B < C	Forward	Reverse	Forward-active
	E < B > C	Forward	Forward	Saturation
	E > B < C	Reverse	Reverse	Cut-off
	E > B > C	Reverse	Forward	Reverse-active
PNP	E < B < C	Reverse	Forward	Reverse-active
	E < B > C	Reverse	Reverse	Cut-off
	E > B < C	Forward	Forward	Saturation
	E > B > C	Forward	Reverse	Forward-active

The Common Base (CB) Configuration as amplifier:



Current amplification factor/current gain:

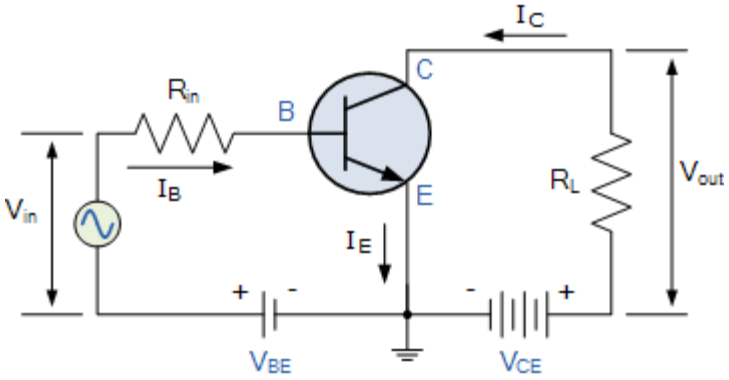
$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}\ =\ \text{constant}}$$

Total collector current in active region:

$$I_C = \alpha I_E + I_{CBO}$$

The Common Emitter Amplifier Circuit



Current amplification factor/current gain:

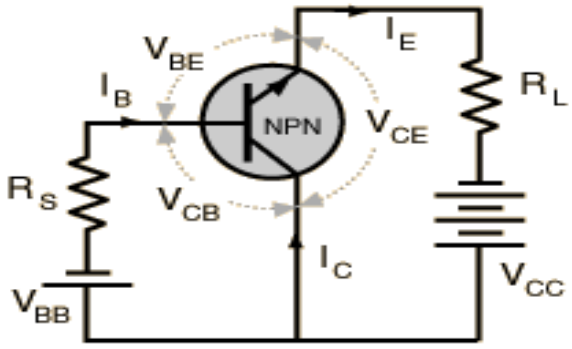
$$\beta_{dc} = \frac{I_C}{I_B}$$

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}}$$

Total collector current in active region:

$$I_C = \beta I_B + I_{CEO}$$

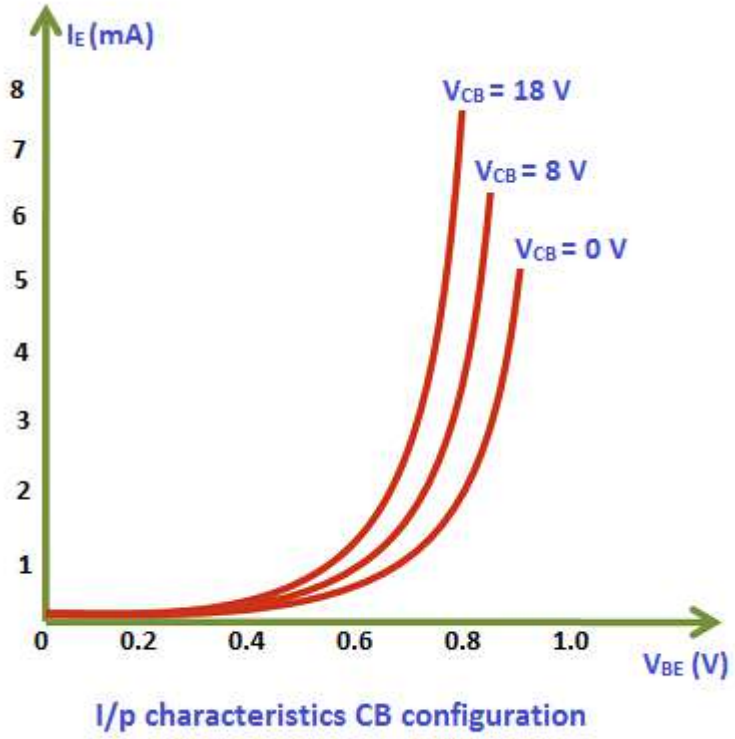
The Common Collector Transistor Circuit



Current amplification factor/current gain:

$\gamma = I_E/I_B$

Input Characteristics of CB:



I/p characteristics CB configuration

For p-n-p transistor, the input current is the emitter current (I_E) and the input voltage is the collector emitter voltage (V_{BE}). As the emitter – base junction is forward biased, therefore the graph of I_E Vs V_{BE} is similar to the forward characteristics of a p-n diode. I_E increases for fixed V_{CB} when V_{BE}increases.

BASE WIDTH MODULATION/EARLY EFFECT:

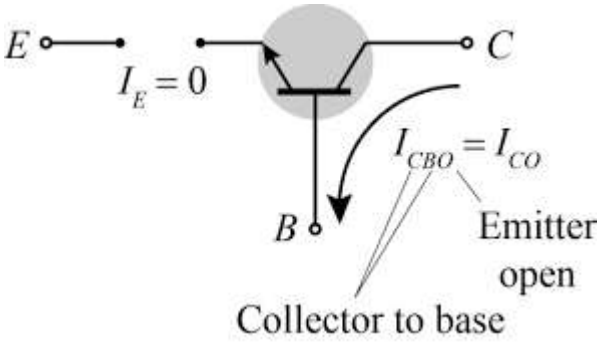
Total base width = width of depletion region at CB junction + width of region which contains free charge carriers

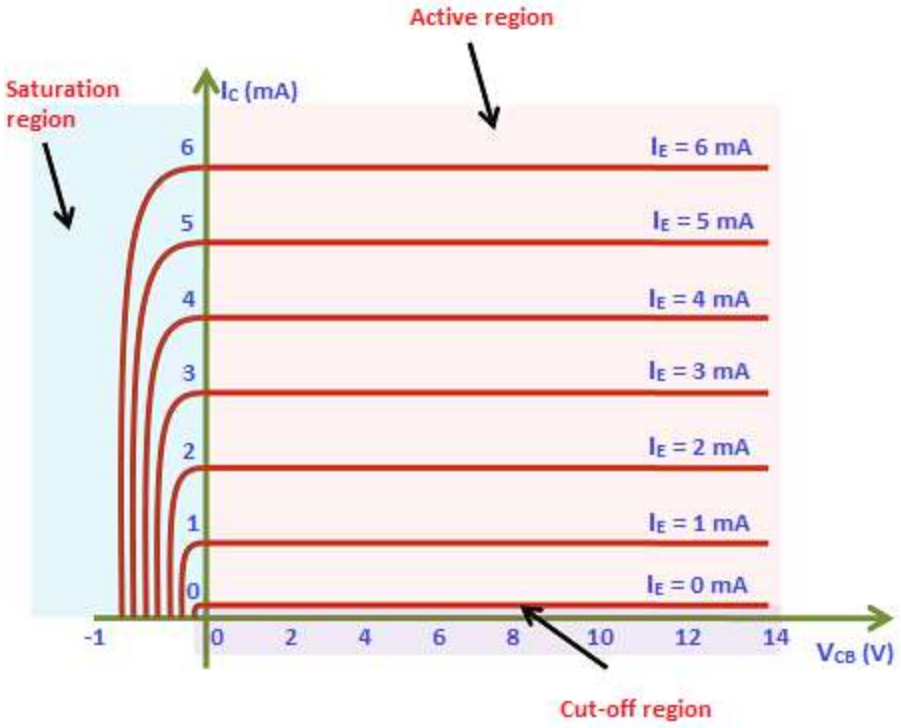
- Due to increase in reverse biasing potential across C-B junction the Input characteristics graph is shifted towards Y-axis or I_E increases.According to dopping base is lightly dopped as compared to collector.
- In N dopped collector majority charge carriers are free electrons,so free electrons will try to move to P dopped Base leaving immobile positive ions near the junction.
- As collector is heavily dopped and due to the presecnce of more free electrons, free electrons in collector will try to fill these immobile positive ions.
- Due to this the width of depletion region across collector decreases and as the base is lightly dopped so the depletion region is shifted more towards the base and the effective width which is responsible for base current will decrease due to the increase in reverse biasing potential across C-B.
- As the effective width of base will decrease then base current will also decrease.
- With the increase in reverse biasing potential the concentration gradient of charge carriers(holes) in the effective width of base will increase and more charge carriers from emitter will try to move to this area and I_E increases.This effect is known as BASE WIDTH MODULATION.

Output Characteristics of CB:

The output characteristics shows the relation between output voltage$V_{CB}$and output current. I_C , here the emitter current I_E is the input current which works as the parameter. CE mode has also three regions named (i) Active region, (ii) cut-off regions, (iii) saturation region.For cutoff region I_E=0 and $I_C = I_{CBO}$ in this region.

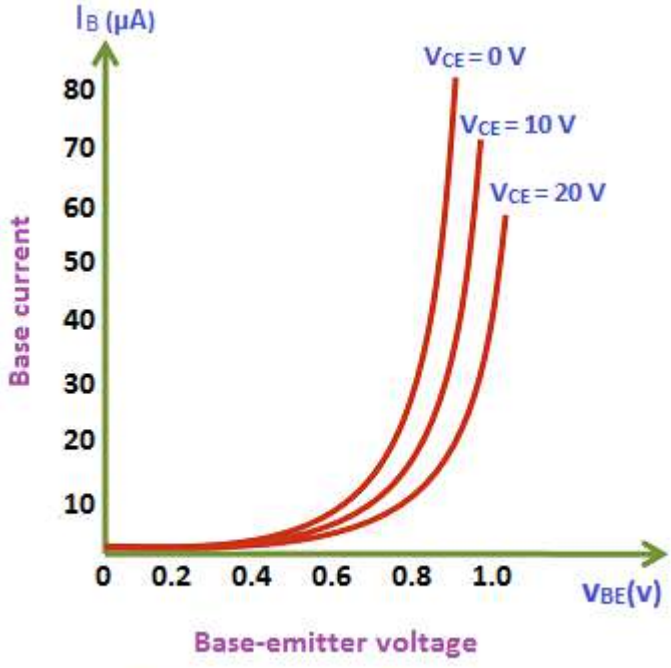
$I_{CBO} = Collector\ to\ base\ current\ when\ emitter\ is\ open$(Due to minority charge carriers)





O/P characteristics CB configuration

Input Characteristics of CE:

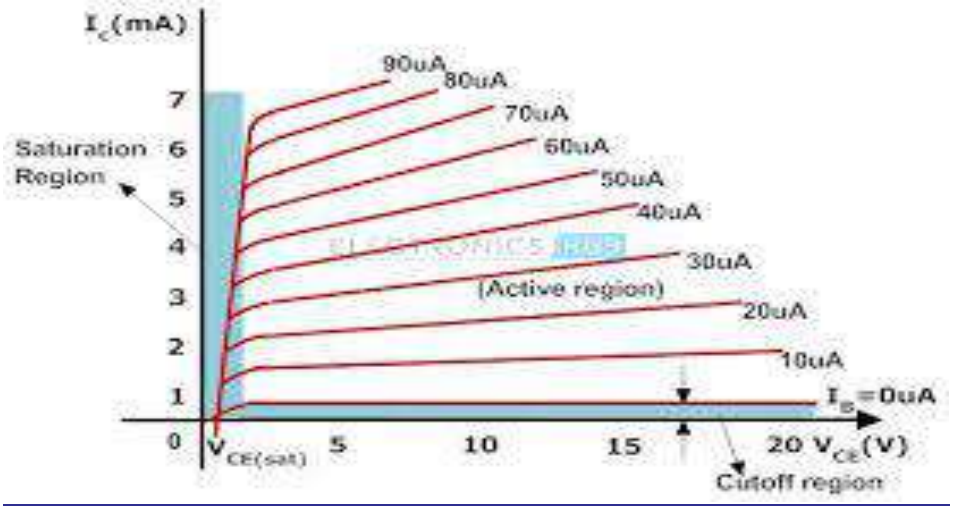


I/P characteristics CE configuration

I_B (Base Current) is the input current, V_{BE} (Base – Emitter Voltage) is the input voltage for CE (Common Emitter) mode. So, the input characteristics for CE mode will be the relation between I_B and V_{BE} with V_{CE} as parameter. The typical

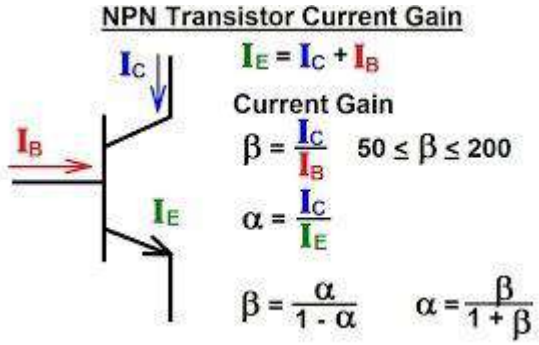
CE input characteristics are similar to that of a forward biased of p-n diode. But as V_{CB} increases the base width decreases.

Output Characteristics of CE:



Output characteristics for CE mode is the curve or graph between collector current (I_C) and collector – emitter voltage (V_{CE}) when the base current I_B is the parameter. Like the output characteristics of common – base transistor CE mode has also three regions named (i) Active region, (ii) cut-off regions, (iii) saturation region. The active region has collector region reverse biased and the emitter junction forward biased. For cut-off region the emitter junction is slightly reverse biased and the collector current is not totally cut-off andI_B=0 and $I_C = I_{CEO}$ in this region. And finally for saturation region both the collector and the emitter junction are forward biased.

$I_{CEO} = Collector\ to\ emitter\ current\ when\ base\ is\ open$(Due to minority charge carriers)



$$I_{CEO} = I_{CBO} / (1-\alpha)$$

TRANSISTOR BIASING

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

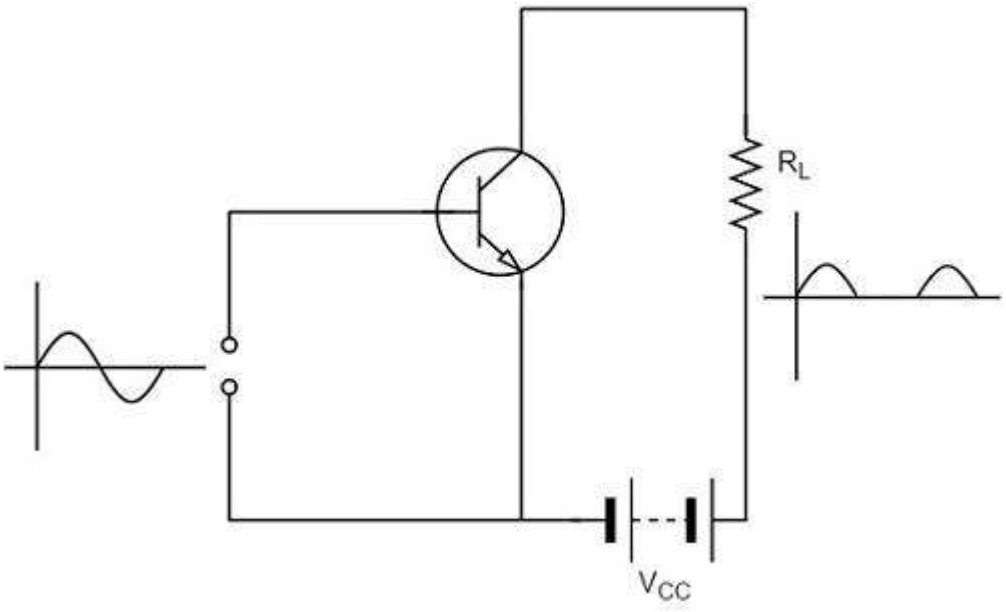
(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

Proper Zero Signal Collector Current

In order to understand this, let us consider a NPN transistor circuit as shown in the figure below. The base-emitter junction is forward biased and the collector-emitter junction is reverse biased. When a signal is applied at the input, the base-emitter junction of the NPN transistor gets forward biased for positive half cycle of the input and hence it appears at the output.

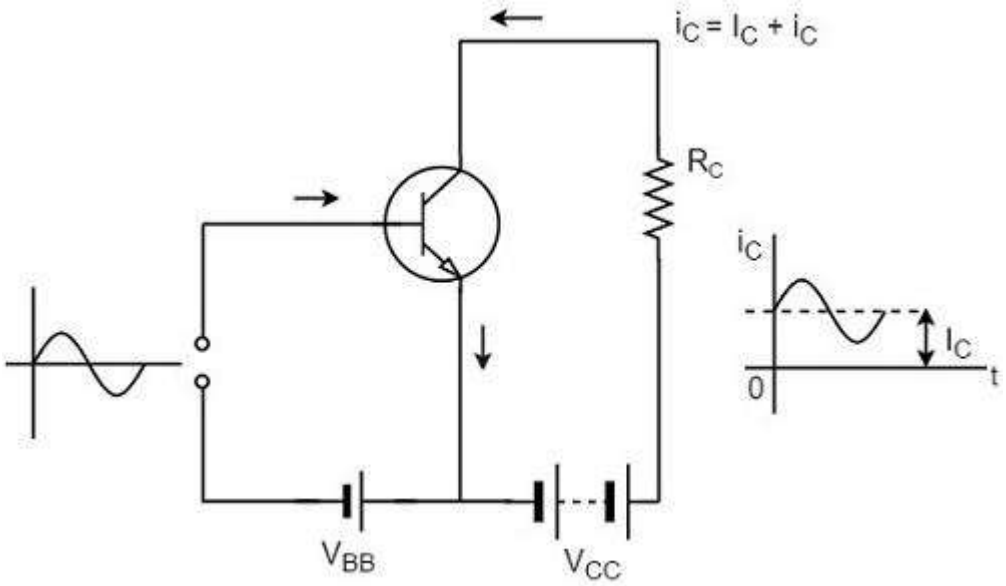
For negative half cycle, the same junction gets reverse biased and hence the circuit doesn't conduct. This leads to **unfaithful amplification** as shown in the figure below.



Let us now introduce a battery V_{BB} in the base circuit. The magnitude of this voltage should be such that the base-emitter junction of the transistor should remain in forward biased, even

for negative half cycle of input signal. When no input signal is applied, a DC current flows in the circuit, due to V_{BB}. This is known as **zero signal collector current** I_C.

During the positive half cycle of the input, the base-emitter junction is more forward biased and hence the collector current increases. During the negative half cycle of the input, the input junction is less forward biased and hence the collector current decreases. Hence both the cycles of the input appear in the output and hence **faithful amplification** results, as shown in the below figure.



Hence for faithful amplification, proper zero signal collector current must flow. The value of zero signal collector current should be at least equal to the maximum collector current due to the signal alone.

Proper Minimum V_{BE} at any instant

The minimum base to emitter voltage $\mathbf{V_{BE}}$ should be greater than the cut-in voltage for the junction to be forward biased. The minimum voltage needed for a silicon transistor to conduct is 0.7v and for a germanium transistor to conduct is 0.5v. If the base-emitter voltage $\mathbf{V_{BE}}$ is greater than this voltage, the potential barrier is overcome and hence the base current and collector currents increase sharply.

Hence if $\mathbf{V_{BE}}$ falls low for any part of the input signal, that part will be amplified to a lesser extent due to the resultant small collector current, which results in unfaithful amplification.

Proper Minimum V_{CE} at any instant

To achieve a faithful amplification, the collector- emitter voltage V_{CE} should not fall below the cut-in voltage, which is called as **Knee Voltage**. If $\mathbf{V_{CE}}$ is lesser than the knee voltage, the collector base junction will not be properly reverse biased. Then the collector cannot attract the electrons which are emitted by the emitter and they will flow towards base which increases the base current. Thus the value of β falls.

Therefore, if $\mathbf{V_{CE}}$ falls low for any part of the input signal, that part will be multiplied to a lesser extent, resulting in unfaithful amplification. So if $\mathbf{V_{CE}}$ is greater than V_{KNEE} the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

TRANSISTOR BIASING, DC LOAD LINE,QUIESCENT POINT

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

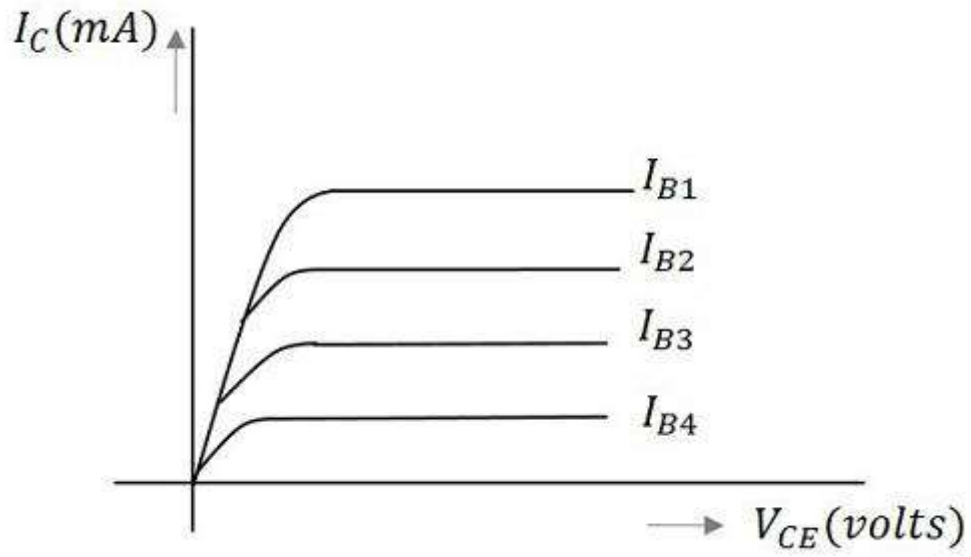
If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values.



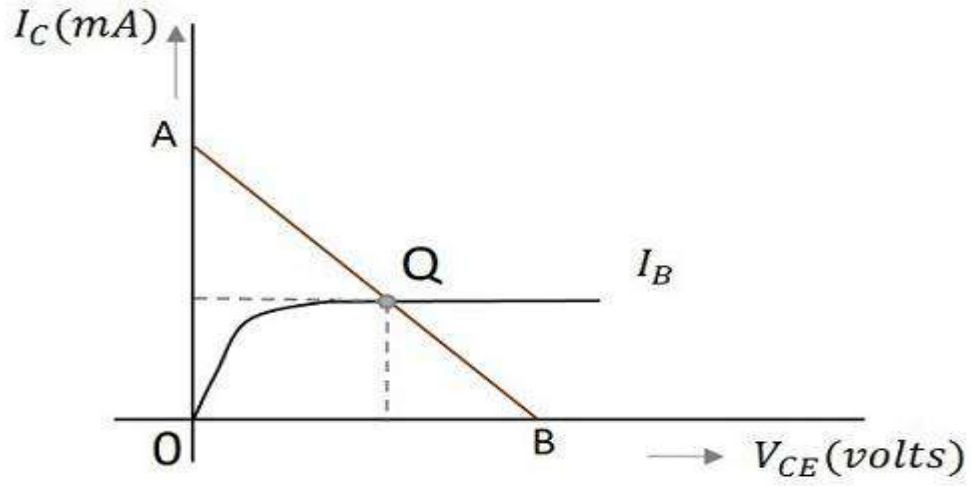
In the above figure, the output characteristics are drawn between collector current $\mathbf{I_C}$ and collector voltage $\mathbf{V_{CE}}$ for different values of base current $\mathbf{I_B}$. These are considered here for different input values to obtain different output curves.

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure below.

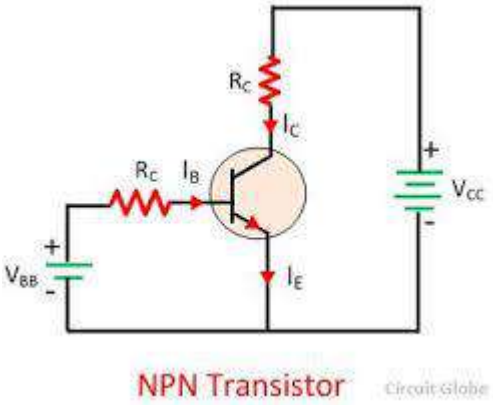


The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

DC Load line

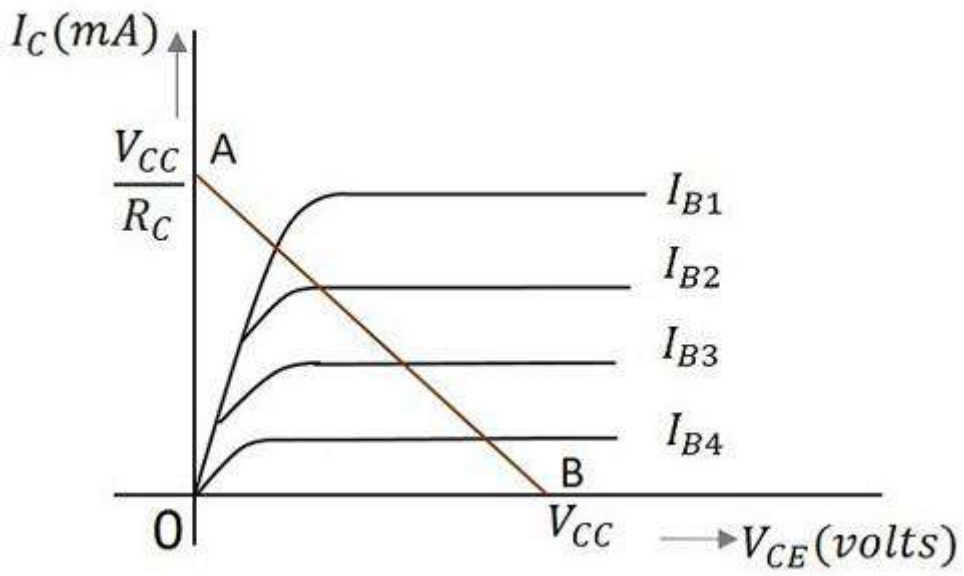
When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition. Here there will be no amplification as the AC signal is absent. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

$$V_{CE}=V_{CC}-I_CR_C$$

As V_{cc} and R_c are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.



To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{CC}/R_C. This gives the maximum value of V_{CE}. This is shown as

$$V_{CE}=V_{CC}-I_CR_C$$

$$0=V_{CC}-I_CR_C$$

$$I_C=V_{CC}/R_C$$

This gives the point A (OA = V_{CC}/R_C) on collector current axis, shown in the above figure.

To obtain B

When the collector current I_C = 0, then collector emitter voltage is maximum and will be equal to the V_{CC}. This is shown as

$$V_{CE}=V_{CC}-I_CR_C$$

$$V_{CE}=V_{CC}$$

(As I_C = 0)

This gives the point B, which means (OB = $\mathbf{V_{cc}}$) on the collector emitter voltage axis shown in the above figure.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

METHODS OF TRANSISTOR BIASING

The biasing in transistor circuits is done by using two DC sources $\mathbf{V_{BB}}$ and $\mathbf{V_{CC}}$. It is economical to minimize the DC source to one supply instead of two which also makes the circuit simple.

The commonly used methods of transistor biasing are

- Base Resistor method
- Emitter stabilised biasing
- Biasing with Collector feedback resistor
- Voltage-divider bias

All of these methods have the same basic principle of obtaining the required value of I_B and I_C from V_{CC} in the zero signal conditions.

Base Resistor Method

In this method, a resistor R_B of high resistance is connected in base, as the name implies. The required zero signal base current is provided by V_{CC} which flows through $\mathbf{R_B}$. The base emitter junction is forward biased, as base is positive with respect to emitter.

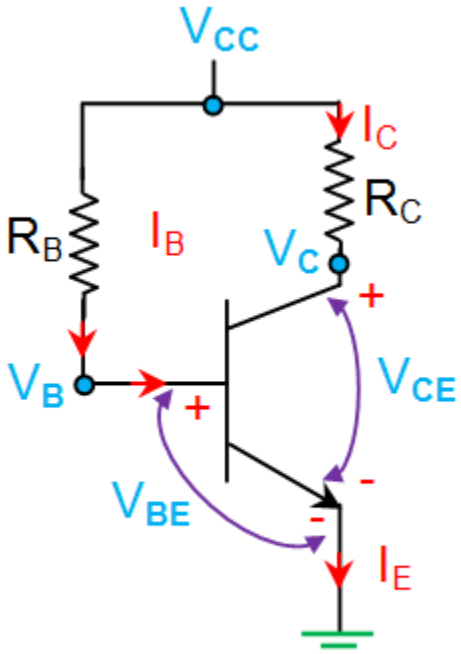


Figure 1 Fixed Base Bias Circuit

The required value of zero signal base current and hence the collector current (as $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor $\mathbf{R_B}$. Hence the value of R_B is to be known. The figure above shows how a base resistor method of biasing circuit looks like.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Let $\mathbf{I_C}$ be the required zero signal collector current=β $\mathbf{I_B}$

We know that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. As R_B can be found directly, this method is called as **fixed bias method**.

Applying KVL at collector to emitter junction or output side:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C$$

In addition, since

$$V_{BE} = V_B - V_E$$

and $V_E = 0$ V, then

$$V_{BE} = V_B$$

Advantages

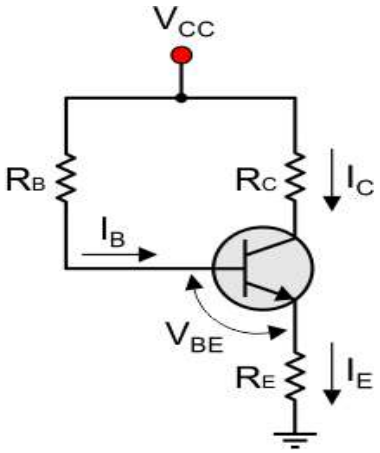
- The circuit is simple.
- Only one resistor $\mathbf{R_B}$ is required.
- Biasing conditions are set easily.
- No loading effect as no resistor is present at base-emitter junction.

Disadvantages

- The stabilization is poor as heat development can't be stopped.
- The stability factor is very high. So, there are strong chances of thermal run away.

Hence, this method is rarely employed.

Emitter stabilised biasing



this biasing circuit is nothing but a fixed bias network with an additional emitter resistor, R_E. Here, if I_C rises due to an increase in temperature, then the I_E also increases which further increases the voltage drop across R_E. This results in the reduction of V_C, causing a decrease in I_B which in turn brings I_C back to its normal value. Thus this kind of biasing network is seen to offer better stability when compared to fixed base bias network. However the presence of R_E reduces the voltage gain of the amplifier as it results in unwanted AC feedback. In this circuit, the mathematical equations for different voltages and current are given as

Applying KVL at I/P loop:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

Putting the value of emitter current:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms will then provide the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1) we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

Collector–Emitter Loop

Applying KVL At output circuit:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

$$\boxed{V_E = I_E R_E}$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$\boxed{V_C = V_{CE} + V_E}$$

or

$$\boxed{V_C = V_{CC} - I_C R_C}$$

The voltage at the base with respect to ground can be determined from

$$\boxed{V_B = V_{CC} - I_B R_B}$$

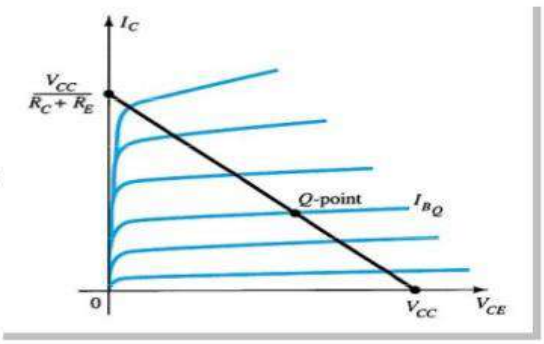
or

$$\boxed{V_B = V_{BE} + V_E}$$

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}}$$

Load-line Analysis

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$V_{CE} = V_{CC}$

$I_C = 0$ mA

I_{Csat}:

$V_{CE} = 0$ V

$I_C = \frac{V_{CC}}{R_C + R_E}$

- Voltage-divider bias:

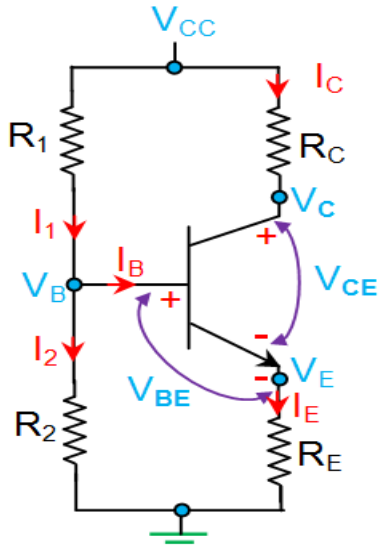


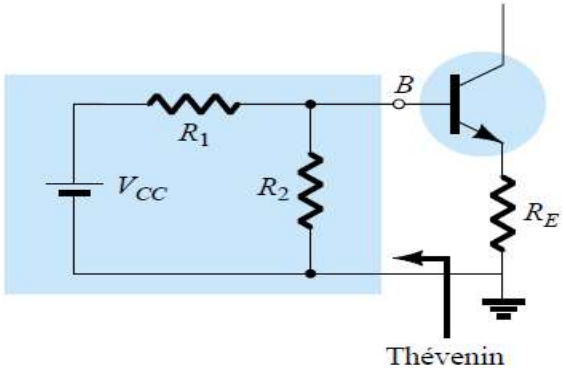
Figure 7 Voltage Divider Bias Circuit

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method* that can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

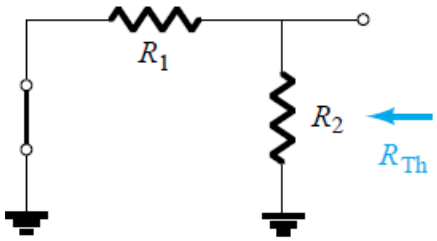
EXACT ANALYSIS:

CONDITION: $\beta R_E < 10R_2$

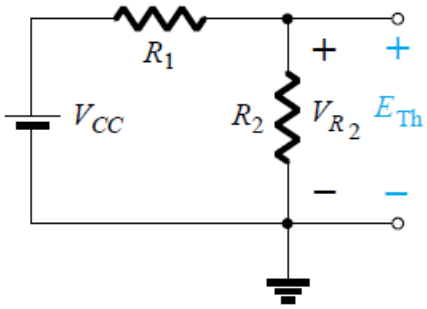


CIRCUIT FOR EXACT ANALYSIS

R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown



$$R_{Th} = R_1 \| R_2$$

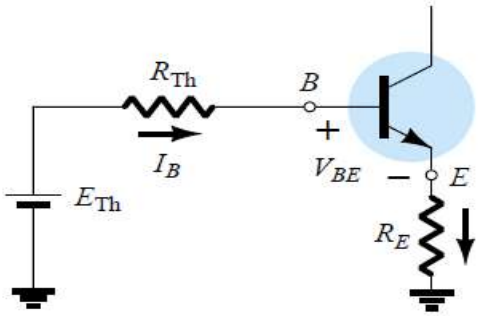


E_{Th}: The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage

Applying the voltage-divider rule:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Applying KVL at the for the input thevenin loop:



$$E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

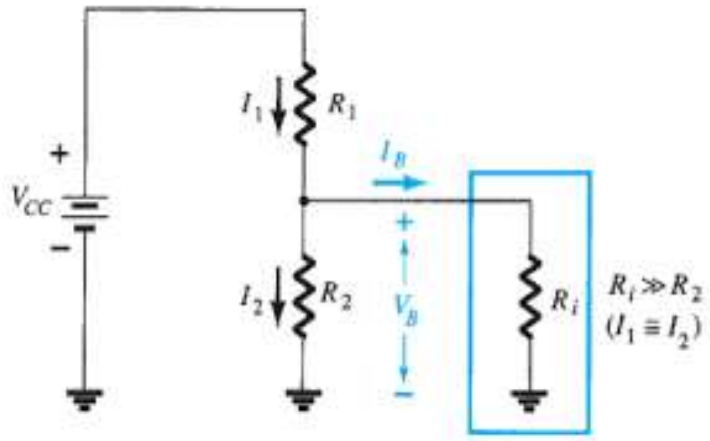
$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

2.APPROXIMATE ANALYSIS:

CONDITION:$\beta R_E \geq 10R_2$



The emitter resistance R_E is seen as $(\beta+1)R_E$ at the input loop.
If this resistance is much higher compared to R_2, then the current I_B is much smaller than I_2 through R_2.
This means, $Ri >> R2$

OR

$(\beta+1)R_E \geq 10R2$

OR

$\beta R_E \geq 10R2$

This makes I_B to be negligible.
Thus I_1 through R_1 is almost same as the current I_2 through R_2.
Thus R_1 and R_2 can be considered as in series.
Voltage divider can be applied to find the voltage across R_2 (V_B)

$$V_B = V_{CC}R_2 / (R_1 + R_2)$$

Once V_B is determined, V_E is calculated as,

$$V_E = V_B - V_{BE}$$

After finding V_E, I_E is calculated as,

$$I_E = V_E / R_E$$
$$I_E \cong I_C$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\ \text{V}}$$

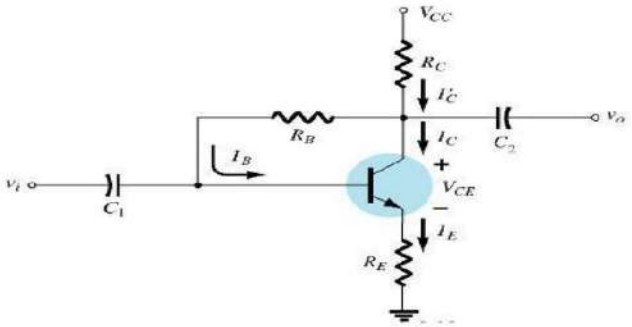
$$V_{CE} = V_{CC}|_{I_C=0\ \text{mA}}$$

ADVANTAGES OF VOLTAGE DIVIDER BIASING:

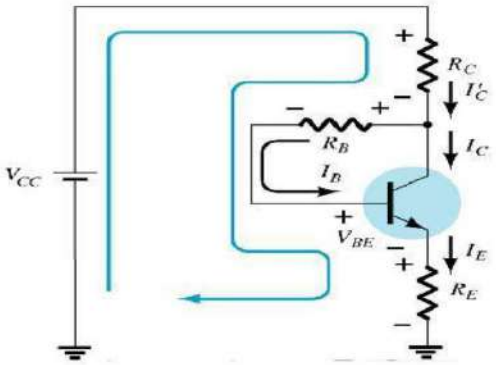
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

- Biasing with Collector feedback resistor

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. below.Although the *Q*-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analysing the base–emitter loop with the results applied to the collector–emitter loop



Input loop



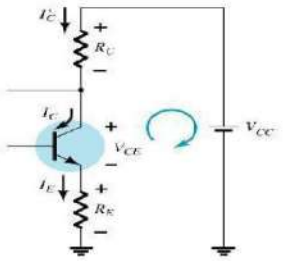
Applying KVL for Input Loop:

$$V_{CC} = I_{C1}R_C + I_BR_B + V_{BE} + I_ER_E$$

Substituting for I_E as $(\beta +1)I_B$ and solving for I_B,

$$I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$$

Output loop



Collector–Emitter Loop

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

Neglecting the base current, KVL to the output loop results in,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Saturation Conditions

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

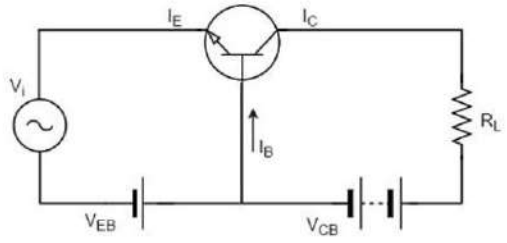
$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} will be defined by the chosen bias configuration.

3. Transistor as an Amplifier

A transistor acts as an amplifier by raising the strength of a weak signal. The DC bias voltage applied to the emitter base junction, makes it remain in forward biased condition. This forward bias is maintained regardless of the polarity of the signal. The below figure shows how a transistor looks like when connected as an amplifier.



The low resistance in input circuit, lets any small change in input signal to result in an appreciable change in the output. The emitter current caused by the input signal contributes the collector current, which when flows through the load resistor R_L, results in a large voltage drop across it. Thus a small input voltage results in a large output voltage, which shows that the transistor works as an amplifier.

Example

Let there be a change of 0.1v in the input voltage being applied, which further produces a change of 1mA in the emitter current. This emitter current will obviously produce a change in collector current, which would also be 1mA.

A load resistance of 5kΩ placed in the collector would produce a voltage of

$$5\ \text{k}\Omega \times 1\ \text{mA} = 5\text{V}$$

Hence it is observed that a change of 0.1v in the input gives a change of 5v in the output, which means the voltage level of the signal is amplified.

BJT as a switch

A bipolar junction transistor (BJT) can be used in many circuit configurations such as an amplifier, oscillator, filter, rectifier or just used as an on-off switch. If the transistor is biased into the linear region, it will operate as an amplifier or other linear circuit, if biased alternately in the saturation and cut-off regions, then it is being used as a switch, allowing current to flow or not to flow in other parts of the circuit. This lab activity describes the BJT when operated as a switch.

Switching circuits are significantly different than linear circuits. They are also easier to understand. Before investigating more complex circuits, we will begin by introducing discrete solid-state switching circuits: those built around BJTs.

A switch consists of a BJT transistor that is alternately driven between the saturation and cutoff regions. A simple version of the switch is shown in figure 1. When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure. When the BJT is in cutoff, the circuit (ideally) has the following values:

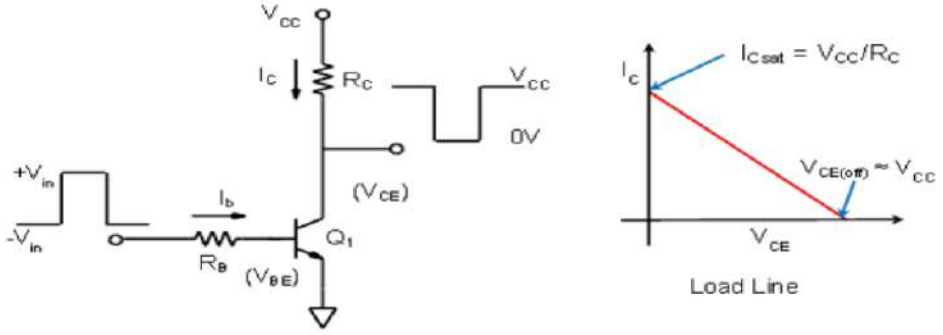
$V_{CE} = V_{CC}$ and $I_C = 0$ A

This state is similar to an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

$V_{CE} \approx 0$V and $I_{Csat} = V_{CC}/R_C$

This state is similar to a closed switch connecting the bottom of R_C to ground.



The characteristics for a BJT switch assume that:

1. $-V_{in}$ is low enough to drive the transistor into cutoff.
2. $+V_{in}$ must produce enough base current through R_B to drive the transistor into saturation.
3. The transistor is an ideal component.

These conditions can be assured by designing the circuit so that:

1. $-V_{in} = V_{BE}$
2. $+V_{in} = V_{BE} + I_B R_B$ (V_{CC} is a good maximum)
3. $I_B > I_{Csat}/ß$

Condition 1 guarantees that the circuit is driven into the cutoff region by the input. Conditions 2 and 3 assure that the transistor will be driven into the saturation region.

An actual BJT switch differs from the ideal switch in several aspects. In practice, even in cutoff there is some leakage current through the transistor. Also, in saturation, there is always some voltage dropped across the

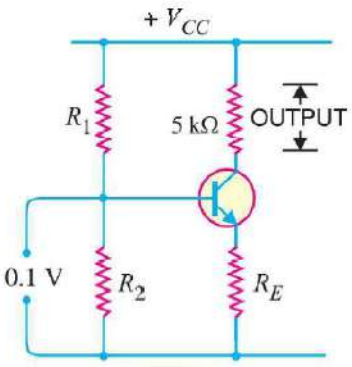
transistor's internal resistance. Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device. These variations from the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analyzing or designing a BJT switch circuit.

SMALL SIGNAL ANALYSIS OF BJT

all electronic equipments must include means for amplifying electrical signals. For instance, radio receivers amplify very weak signals—sometimes a few millionth of a volt at antenna–until they are strong enough to fill a room with sound. The transducers used in the medical and scientific investigations generate signals in the microvolt (μV) and millivolt (mV) range. These signals must be amplified thousands and millions times before they will be strong enough to operate indicating instruments. Therefore, electronic amplifiers are a constant and important ingredient of electronic systems.

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as **single stage transistor amplifier.**

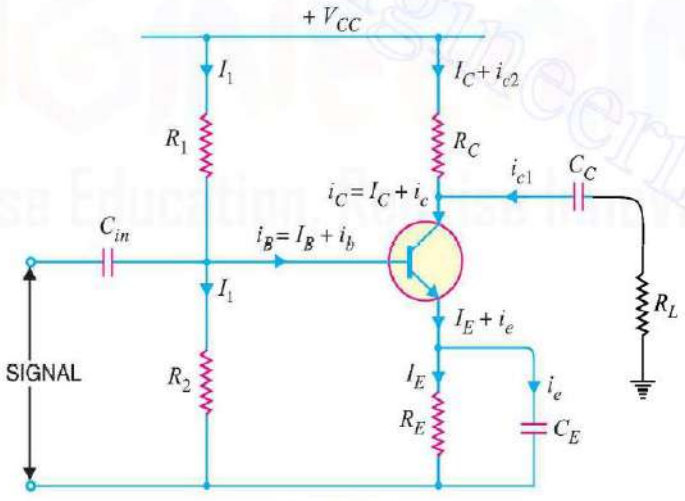
A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components. Although a practical amplifier consists of a number of stages, yet such a complex circuit can be conveniently split up into separate single stages. By analysing carefully only a single stage and using this single stage analysis repeatedly, we can effectively analyse the complex circuit. It follows, therefore, that single stage amplifier analysis is of great value in understanding the practical amplifier circuits.



PRACTICAL CIRCUIT OF TRANSISTOR AMPLIFIER:

(*i*) Biasing circuit. The resistances R_1, R_2 and R_E form the biasing and stabilisation circuit. The biasing circuit must establish a proper operating point otherwise a part of the negative half-cycle of the signal may be cut off in the output.

(*ii*) Input capacitor C_{in}. An electrolytic capacitor C_{in} ($\simeq 10\ \mu F$) is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R_2 and thus change the bias. The capacitor C_{in} allows only a.c. signal to flow but isolates the signal source from R_2.*



***(iii)* Emitter bypass capacitor C_E.** An emitter bypass capacitor C_E ($\simeq 100\mu F$) is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.

***(iv)* Coupling capacitor C_C.** The coupling capacitor C_C ($\simeq 10\mu F$) couples one stage of ampli-

* It may be noted that a capacitor offers infinite reactance to d.c. and blocks it completely whereas it allows a.c. to pass through it.

CURRENTS IN TRANSISTOR AFTER APPLICATION OF AC SIGNAL:

***(i)* Base current.** When no signal is applied in the base circuit, d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by:

$$i_B = I_B + i_b$$

***(ii)* Collector current.** When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, a.c. collector current i_c also flows. Therefore, the total collector current i_C is given by:

$$i_C = I_C + i_c$$

where $I_C = \beta I_B$ = zero signal collector current

$i_c = \beta i_b$ = collector current due to signal.

***(iii)* Emitter current.** When no signal is applied, a d.c. emitter current I_E flows. With the application of signal, total emitter current i_E is given by :

$$i_E = I_E + i_e$$

It is useful to keep in mind that :

$$I_E = I_B + I_C$$

$$i_e = i_b + i_c$$

Now base current is usually very small, therefore, as a reasonable approximation,

$$I_E \simeq I_C \quad \text{and} \quad i_e \simeq i_c$$

IMPORTANT POINTS:

The following points regarding the input / output phase relationships between currents and voltages for the various transistor configurations may be noted :

(*i*) *For every amplifier type (CE, CB and CC), the input and output currents are in phase.* When the input current decreases, the output current also decreases and vice-versa.

(*ii*) *Remember that common emitter (CE) circuit is the* ***only configuration*** *that has input and output voltages 180° out of phase.*

(*iii*) For both common base (*CB*) and common collector (*CC*) circuits, the input and output voltages are in phase. If the input voltage decreases, the output voltage also decreases and vice-versa.

BJT TRANSISTOR MODELING

The key to the small-signal approach is the use of ac equivalent circuits or models. Here are two models discussed.

- Re-MODEL
- HYBRID-Π MODEL

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of BJT under specific operating conditions**,** In summary the ac equivalent circuit of BJT amplifier is obtained by:

1- Setting all dc sources to zero-potential equivalent and replacing them by a short circuit connection to ground.

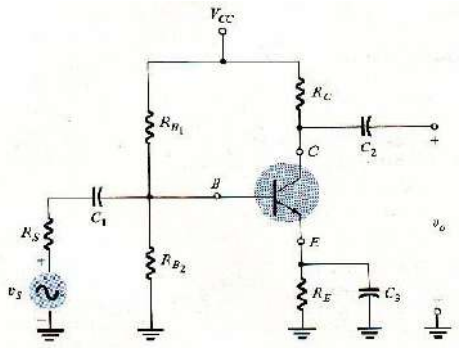


Fig 5-1 Transistor circuit under examination

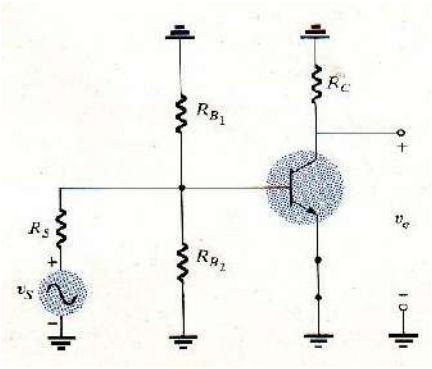


Fig 5-2 the network of Fig5-1 the short circuit equivalent

2-replacing all capacitors short circuit equivalent.
3-Removing all element bypassed by the short circuit equivalents introduced by steps 1 & 2
4-Redrawing the circuit in a more convenient and logical forms (Fig5-3).

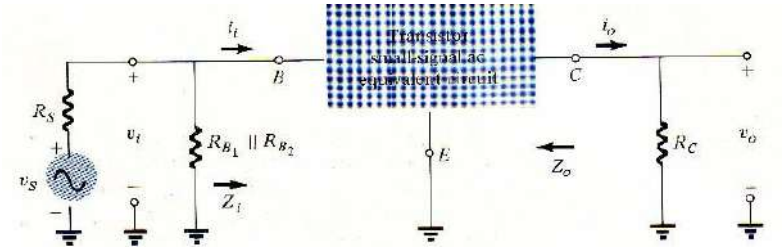


Fig 5-3 small-signal ac analysis ***5- use the hybrid or re equivalent circuit of the BJT to complete the equivalent circuit of the amplifier***

6- Finally, the following important parameters are determined for the amplifier:

1- **Input impedance Z_i**
2- **Output impedance Z_o**
3- **Voltage gain A_v**
4-Current gain A_i
5-phase relationship (θ)

The r_e Transistor Model

The **r_e** model employs a **diode** and controlled **current source** to duplicate the behavior of a transistor. A current-controlled current Sources is one where the parameters of the current source are controlled by a current else where in the network, in general **BJT transistor amplifiers are referred to as current-controlled device.**

Common-Base Configuration (CB)

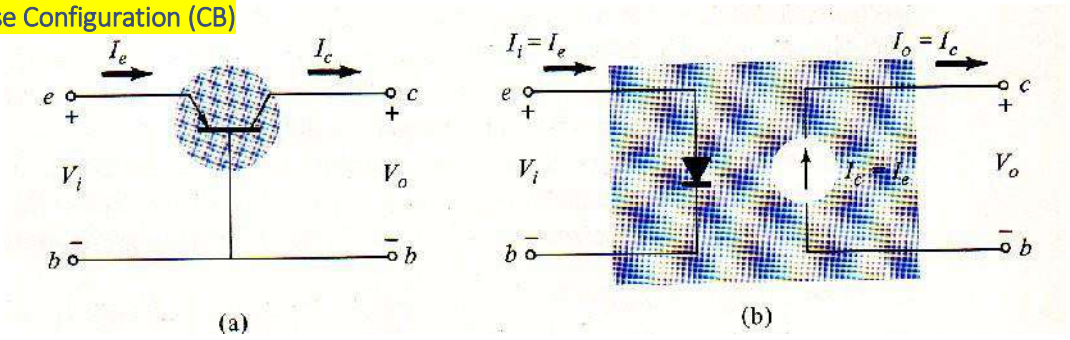


*Fig 5-4(a) CB BJT transistor (b) **r_e** Model for the configuration of (a)*

. ac resistance of a diode can be determined by the equation r_{ac}=26mV / I_D

Same equation can be used to find the ac resistance of the diode of Fig5-4(a) if we simply substitute the emitter current as follows:

$$r_e = \frac{26\text{ mV}}{I_E}$$

e of r_e was chosen to emphasize that it is the dc level of emitter current that determines the ac level of the resistance of the diode of Fig 5-4(b). Substituting the resulting value of r_e in Fig 5- 4(b) will result in the very useful model of fig 5-5

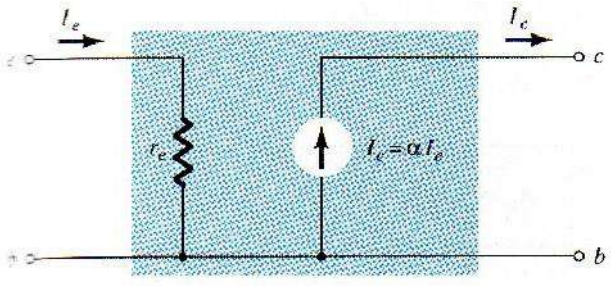


*Fig 5-5 CB **r_e** equivalent circuit*

$$Z_i = r_e \quad CB$$

For the CB, Z_i range from a few ohms to a maximum of about 50 Ω

If we set the signal to zero (V_i=0) then **I_e = 0**A and **I_c = αI_e** = α (0A) = **0A**,Resulting in an open-circuit equivalence at the output terminals

$$Z_o \cong \infty\ \Omega \quad CB$$

For the CB configuration, values of Z_o are in MΩ range for CB the input impedance is relatively small and the output impedance quite high

$$V_o = -I_c R_L = -(-I_c)R_L = \alpha I_e R_L$$

and $$V_i = I_e Z_i = I_e r_e$$

so that $$A_v = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

and $$\boxed{A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}}_{CB} \qquad [5\text{-}1]$$

$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = -\frac{\alpha I_e}{I_e}$$

and $$\boxed{A_i = -\alpha \cong -1}_{CB} \qquad [5\text{-}2]$$

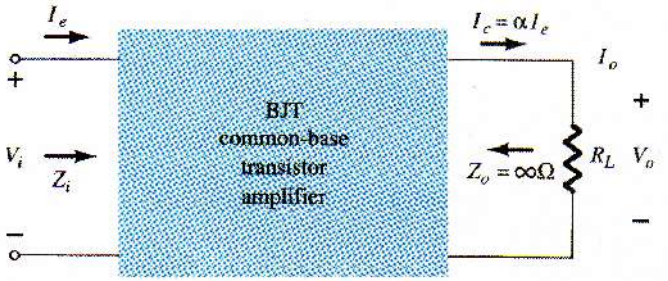


Fig 5-6 ***$A_v = V_o/V_i$*** *for CB*

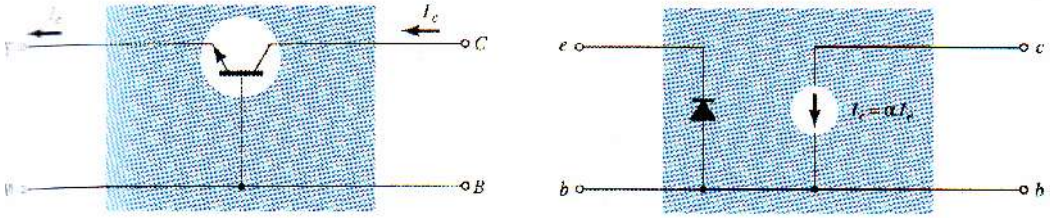


Fig 5-7 approximate model for a CB npn transistor configuration

Example 3: CB configuration with I_E=4mA, α=0.98, and an ac of 2mV applied between the base and emitter. Determine the $\mathbf{Z_i}$. Calculate A_v if a load of 0.56kΩ is connected to the output terminals, find the $\mathbf{Z_o}$ and $\mathbf{A_i}$

Solution:

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = \mathbf{6.5\ \Omega}$$

$$I_i = I_e = \frac{V_i}{Z_i} = \frac{2\text{ mV}}{6.5\ \Omega} = 307.69\ \mu\text{A}$$

$$V_o = I_c R_L = \alpha I_e R_L = (0.98)(307.69\ \mu\text{A})(0.56\text{ k}\Omega)$$

$$= 168.86\text{ mV}$$

$$A_v = \frac{V_o}{V_i} = \frac{168.86\text{ mV}}{2\text{ mV}} = \mathbf{84.43}$$

$$A_v = \frac{\alpha R_L}{r_e} = \frac{(0.98)(0.56\text{ k}\Omega)}{6.5\ \Omega} = \mathbf{84.43}$$

$$Z_o \cong \infty\ \Omega$$

$$A_i = \frac{I_o}{I_i} = -\alpha = \mathbf{-0.98}$$

Common-Emitter Configuration (CE)

For the CE configuration the emitter is common between input and output ports of amplifier. Substituting the $\mathbf{r_e}$ equivalent ckt for npn transistor will result in fig5-8, $\mathbf{I_B}$ is the input current while $\mathbf{I_C}$ is the output current

$$I_c = \beta I_b$$

$$I_e = I_c + I_b = \beta I_b + I_b$$

$$I_e = (\beta + 1) I_b$$

$$I_e \cong \beta I_b \qquad [5\text{-}3]$$

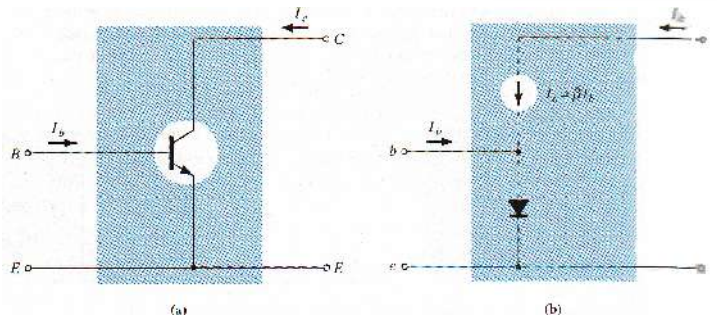


Fig5-8(a) CE BJT (b) approximate model

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$

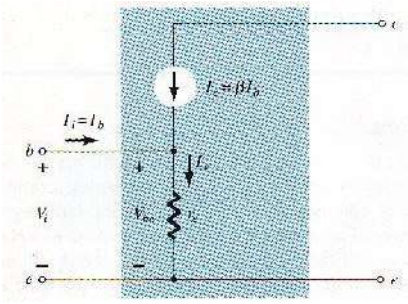


Fig 5-9 ***Z_i*** *using*

$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b} \qquad [5\text{-}4]$$

$$Z_i \cong \beta r_e \quad CE$$

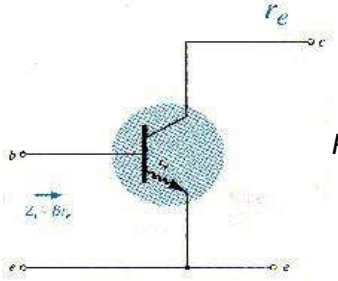


Fig5-10 ***r_e*** *on input impedance*

For the CE configuration $\mathbf{Z_i}$ defined by $\boldsymbol{\beta r_e}$ ranges from a few hundred ohms to the kΩ range, with maximums of about 6-7 kΩ

$$Z_o = r_o \quad CE \qquad [5\text{-}5]$$

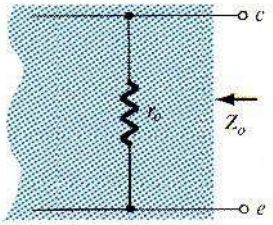


Fig 5-11 ***r_o*** *equivalent circuit*

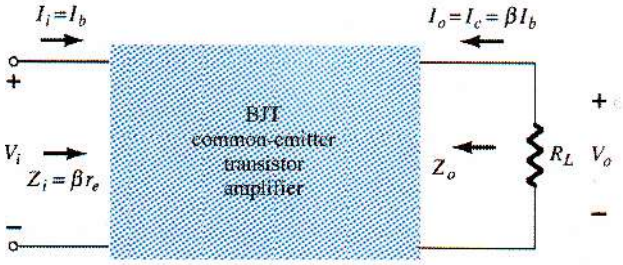


Fig 5-12 Determining A_v & A_i for the CE

$$V_o = -I_o R_L = -I_c R_L = -\beta I_b R_L$$

and $$V_i = I_i Z_i = I_b \beta r_e$$

so that $$A_v = \frac{V_o}{V_i} = -\frac{\beta I_b R_L}{I_b \beta r_e}$$

and $$\boxed{A_v = -\frac{R_L}{r_e}} \quad CE, r_o = \infty\,\Omega \qquad [5\text{-}6]$$

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

$$\boxed{A_i = \beta} \quad CE, r_o = \infty\,\Omega \qquad [5\text{-}7]$$

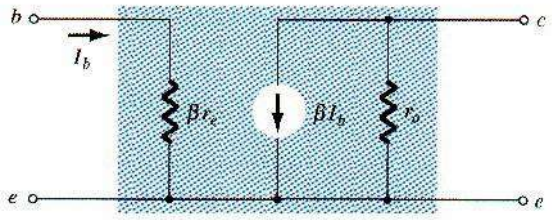


Fig5-13 ***r_e*** *model for the CE configuration*

Example 4: *β=120 and I_E=3.2mA for CE configuration with* ***r_o=∞Ω****, determine*

(a) Z_i.
(b) A_v if a load of 2 kΩ is applied.
(c) A_i with the 2 kΩ load.

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{3.2\text{ mV}} = 8.125\ \Omega$$

$$\text{and } Z_i = \beta r_e = (120)(8.125\ \Omega) = \mathbf{975\ \Omega}$$

$$A_v = -\frac{R_L}{r_e} = -\frac{2\text{ k}\Omega}{8.125\ \Omega} = \mathbf{-246.15}$$

$$A_i = \frac{I_o}{I_i} = \beta = \mathbf{120}$$

Common-Collector Configuration (CC)

For the CC configuration the model of CE configuration is normally applied.

The Hybrid (h-parameter) Equivalent Model

r_e model for the transistor is sensitive to the dc level of operation of the amplifier. For the hybrid equivalent model the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier.

For the basic three-terminal electronic device there are two ports (pairs of terminals) of interest. The set **at the left** will represent the **input terminals**, and the set at **the right, the output terminals.**

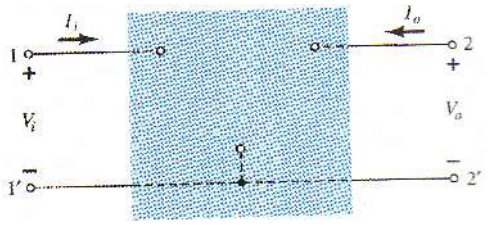


*Fig5-14 Two port system For each set of terminals, there **are two variables of interest***

$$V_i = h_{11}I_i + h_{12}V_o \qquad [5\text{-}8a]$$

$$I_o = h_{21}I_i + h_{22}V_o \qquad [5\text{-}8b]$$

The parameters relating the four variables are called h-parameters from the word hybrid (V& I)

Set $V_o=0$(short circuit the output terminals) and solve Eq[5-8a] for h_{11}

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} \quad \text{ohms}$$

$=h_i(\Omega)$ short circuit input impedance parameter

Set I_i equal to zero by opening the input, the following will result for h_{12}

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} \quad \text{unitless}$$

$=h_r$ open circuit reverse transfer voltage ratio

Eq[5-8b] $V_o=0$ by shorting the output terminals, will result for h_{21}

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \quad \text{unitless}$$

$=h_f$ short cct forward transfer current ratio

Again opening the input leads by set $I_i=0$ and solving for h_{22}

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \quad \text{siemens}$$

$=h_o(S)$ open-circuit output admittance

*Since each term of Eq[5-8a] has the unit **volt,** let us apply **KVL in reverse** to find a circuit that fits the equation as in shown Fig5-15*

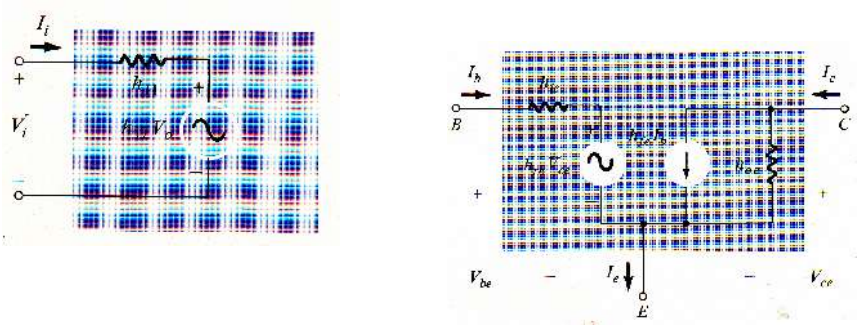


Fig5-15 Hybrid input equivalent circuit

*Since each term of Eq[5-16b] has the units of **current**, let us now apply **KCL in reverse** to obtain the circuit of Fig5-16*

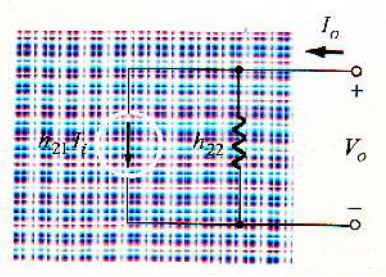


Fig5-16 Hybrid output equivalent circuit.

The complete **ac equivalent circuit** for the basic three-terminal linear device is indicated in Fig5-17 with a new set of subscripts for the h-parameters.

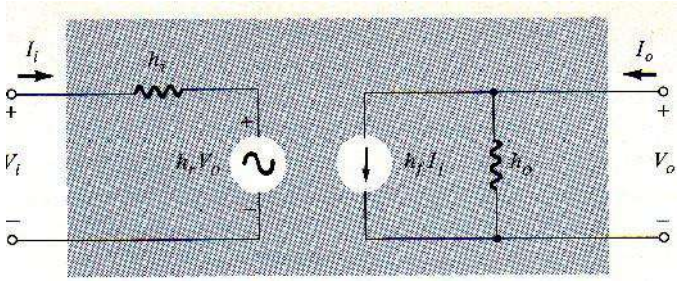


Fig5-17 complete hybrid equivalent circuit

$h_{11} \rightarrow$ input resistance $\rightarrow h_i$

$h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_r$

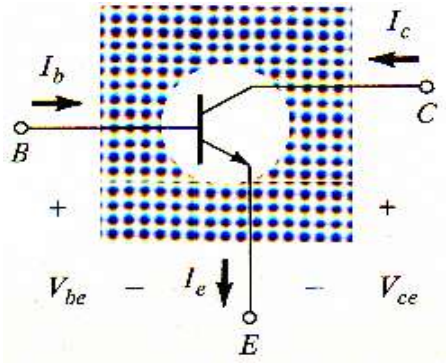
$h_{21} \rightarrow$ forward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ output conductance $\rightarrow h_o$

The circuit of Fig5-17 is applicable to any linear three-terminal electronic device or system with no internal independent sources.

Common Emitter Configuration (CE)

The hybrid equivalent network for the CE configuration is shown Fig5-18,



Note :

$I_i = I_b$

$I_o = I_c$

$V_i = V_{be}$

$V_o = V_{ce}$

Fig5-18 CE configuration, (a) graphical symbol (b) hybrid

Common Base Configuration (CB)

The hybrid equivalent network for the CB configuration is shown Fig5-19, Note that:

$I_i = I_e$

$I_o = I_c$

$V_i = V_{eb}$

$V_o = V_{cb}$

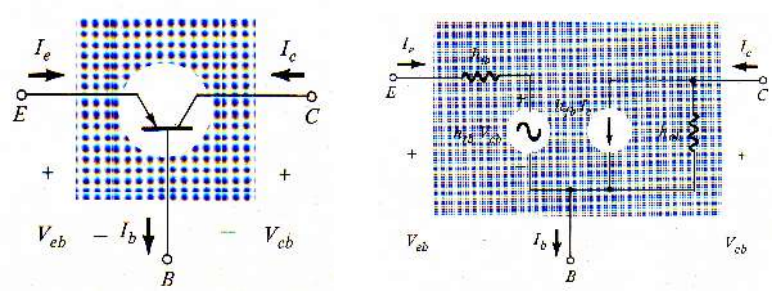


Fig5-19 CB configuration (a) graphical symbol (b) hybrid

The networks of Figs 5-18 & 5-19 are applicable for pnp or npn transistors. There are three different sets of h-parameters (Table 5-1).

	BJT configuration	h-parameters sets
1	Common-Emitter	h_{ie} , h_{fe} , h_{re} , h_{oe}
2	Common-Collector	h_{ic} , h_{fc} , h_{rc} , h_{oc}
3	Common-Base	h_{ib} , h_{fb} , h_{rb} , h_{ob}

Table5-2 lists typical parameter values in each of the three transistor configurations

h-parameters	*CE*	*CC*	*CB*
h_i	1kΩ	1kΩ	20kΩ
h_r	2.5×10^{-4}	≈ 1	3.0×10^{-4}
h_f	50	−50	−0.98
h_o	25 μS	25 μS	0.5 μS
$1/h_o$	40 kΩ	40 kΩ	2 MΩ

Approximate CE & CB hybrid equivalent circuit

Since **h_{re} & h_{rb} are normally small quantity**, their **removal** is approximated by **h_{re} ~ 0** and **$h_{re}V_o$ = 0**, resulting in a **short-circuit** equivalent for the feedback element as shown in Fig5-20 The resistance determined by **$1/h_{oe}$ & $1/h_{ob}$** are **large enough** to be **ignored,** in comparison to a parallel load, which can be replaced by an **open circuit** equivalent for the CE and CB models,

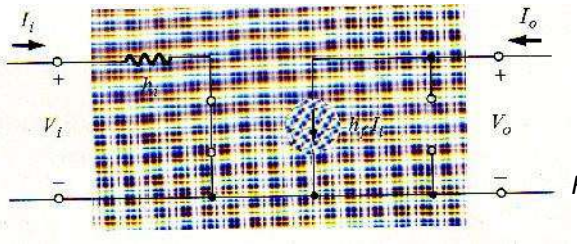


*Fig5-20 Effect of removing **h_{re} & h_{oe}***

The resulting equivalent circuit (fig5-21) is quite similar to the general structure of the CB & CE

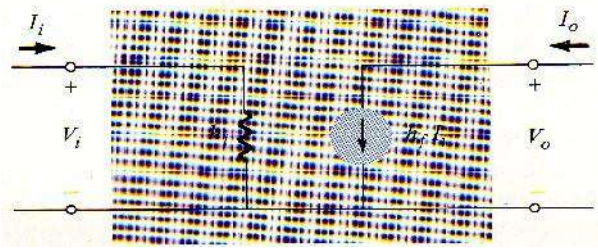
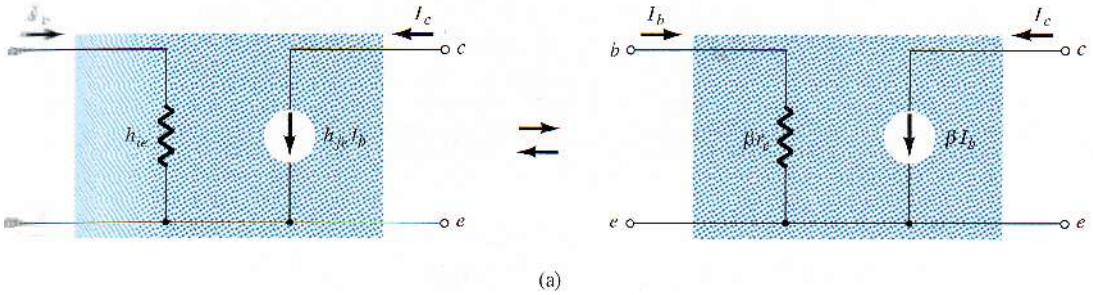
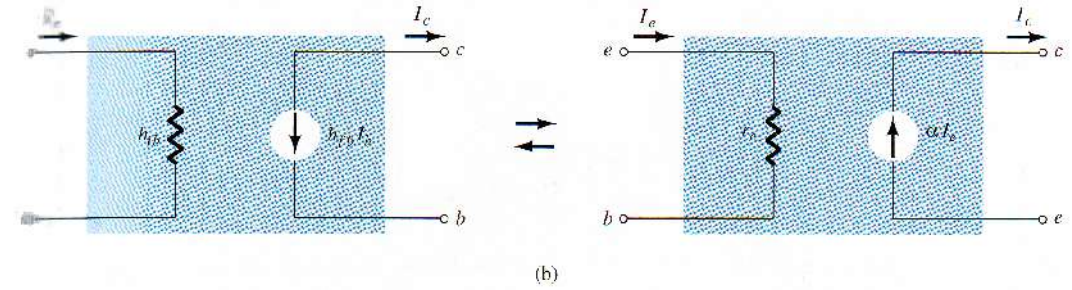


*Fig5-21 approximate **hybrid** model*



(a)

Hybrid versus r_e model CE configuration



(b)

Hybrid versus r_e model CB configuration

Fig5-22 Hybrid versus r_e model (a) CE configuration (b) CB configuration

$$h_{ie} = \beta r_e \qquad [5\text{-}9]$$

$$h_{fe} = \beta_{ac} \qquad [5\text{-}10]$$

$$h_{ib} = r_e \qquad [5\text{-}11]$$

$$h_{fb} = -\alpha \cong -1 \qquad [5\text{-}12]$$

*Note that the minus sign in Eq[5-12] account for the fact that **the current source of the standard hybrid equivalent circuit is pointing down** rather than in the actual direction as shown in the **r_e** model of fig 5-22b*

Example 5:

Given $I_E = 2.5$ mA, $h_{fe} = 140$, $h_{oe} = 20\ \mu$S (μmho), and $h_{ob} = 0.5\ \mu$S, determ
(a) The common-emitter hybrid equivalent circuit.
(b) The common-base r_e model.

Solution:

$$\text{(a)}\quad r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.5\text{ mA}} = 10.4\ \Omega$$

$$h_{ie} = \beta r_e = (140)(10.4\ \Omega) = \mathbf{1.456\ k\Omega}$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

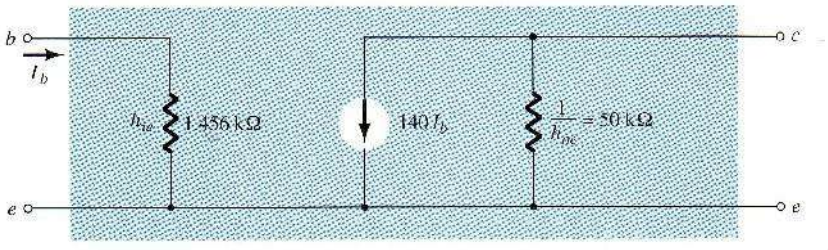


Fig5-23 CE hybrid ckt for Ex 5:

(b) $r_e = 10.4\ \Omega$

$$\alpha \cong 1, \qquad r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\ \mu S} = 2\ M\Omega$$

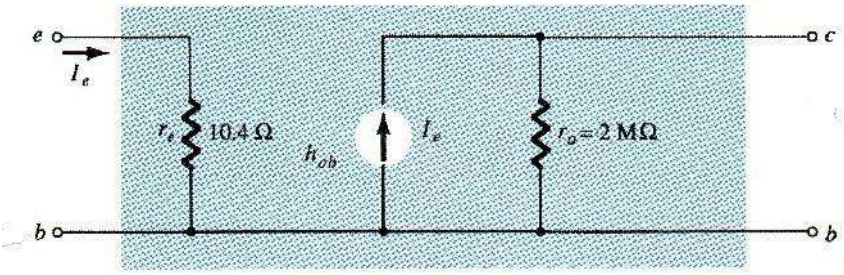


Fig5-24 CB ***r*****e** *model of Ex 5:*

SUMMARY

1- Amplification in the ac domain cannot be obtained without the application of dc biasing level.

2- For most applications the BJT amplifier can be considered linear, permitting the use of the superposition theorem to separate the dc and ac analyses and designs.

3- A model is the combination of circuit elements, carefully chosen, that best approximates the behavior of a BJT for a particular set of operating conditions.

4- When introducing the ac model for a BJT:

a. all dc sources are set to zero and replaced by a short circuit connection to ground.

b. all capacitors are replaced by a short-circuit equivalent.

c. all elements in parallel with an introduced short-circuit equivalent should be removed from the network.

d. the network should be redrawn as often as possible.

5- The input impedance of an ac network cannot be measured with an ohm-meter.

6- The output impedance of an amplifier is measured with the applied signal set to zero. It cannot be measured with an ohmmeter.

7- For all transistor amplifiers, the no-load gain is always greater than the loaded gain.

8- The gain from source to load is always reduced by the internal resistance of the source

9- The current gain of an amplifier is very sensitive to the input impedance of the amplifier and the applied load.

10- The re model for a transistor is very sensitive to the dc biasing network of the amplifier.

11- An output impedance for the re model can be included only if obtained from a data sheet or from a graphical measurement from the characteristic curves.

12- For the common-base configuration, the input impedance is generally quite small and the output impedance quite large. In addition, the voltage gain can be quite large, but the current gain is always very close to 1.

13- For the common-emitter configuration, the input impedance generally is approximately a few kilohms, and the output impedance is relatively large. In addition, the common-emitter configuration can a have a relatively high voltage and current gain.

14- The parameters of a hybrid equivalent model for a transistor are provided for a particular set of dc operating conditions. However, four parameters are provided rather than the two that normally appear for the re model. For some applications the reverse transfer voltage ratio and the typical output impedance normally found in the re model can be quite important.

Equation

$$r_e = \frac{26\ \text{mV}}{I_E}$$

Common-base:

$$Z_i = r_e$$

$$A_v \cong \frac{R_L}{r_e}$$

$$A_i \cong -1$$

Common-emitter:

$$Z_i \cong \beta r_e$$

$$A_v = -\frac{R_L}{r_e}$$

$$A_i = \beta$$

Hybrid:

$$h_{ie} = \beta r_e$$

$$h_{fe} = \beta_{ac}$$

$$h_{ib} = r_e$$

$$h_{fb} = -\alpha \cong -1$$

6-BJT small signal Analysis

1-Common-Emitter Fixed-Bias Configuration (CE)

Input signal V_i is applied to the base of the transistor , recognized that the input current I_i is not the base current but the source current, while the output current I_o is the collector current.
The small-signal ac analysis begins by:

1- Removing the dc effects of V_{cc} and replacing the dc blocking capacitors C_I and C_2 by short- circuit equivalents, resulting in the network of Fig6-2.
Note in Fig6-2 that the common ground of the dc supply and the emitter resistor **permits** the relocation of R_B and R_C in parallel with the input and output sections of the transistor

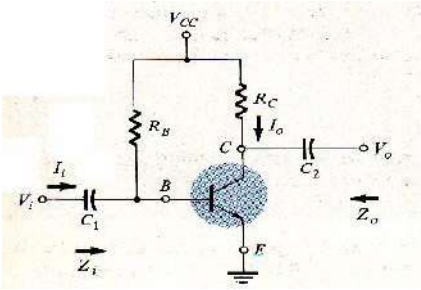


Fig 6-1CE fixed bias configuration

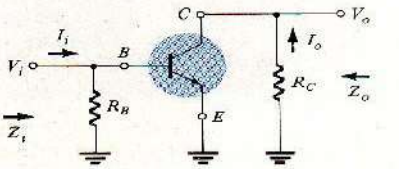


Fig6-2 removal of effects of V_{CC}, C_1, C_2

2-Substituting the approximate r_e small-signal equivalent circuit for the transistor of Fig6-2 will result in the network of Fig6-3 performing following results

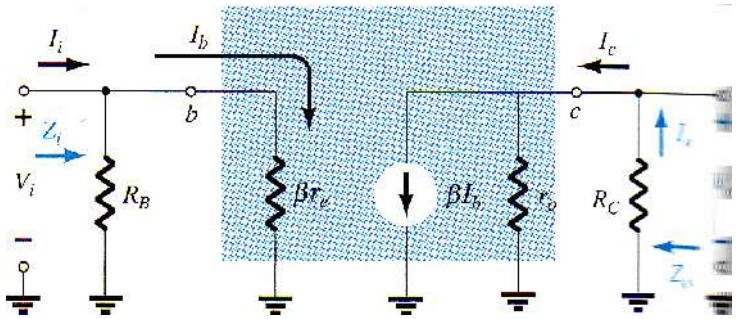


Fig6-3 r_e model to the network

3- The next step is to determine β, r_e, and r_o
The magnitude of **β** obtained from a specification sheet
The magnitude of r_e determine from a dc analysis of the system The magnitude of r_o obtained from a specification sheet
Z_i from fig6-3

$$Z_i = R_B \| \beta r_e \quad \text{ohms} \qquad [6\text{-}1]$$

If R_B>>10 βr_e *then*

$$Z_i \cong \beta r_e \quad \text{ohms} \qquad [6\text{-}2]$$

$R_B \geq 10\beta r_e$

Z_o Determined when V_i=0 , I_i = I_b=0 , resulting in an open-circuit equivalence for the current source, the result is shown in fig 6-4

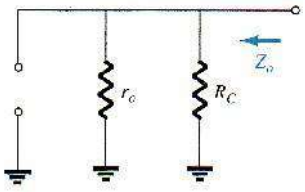


Fig6-4 Determining Z_o for the network

$$Z_o = R_C \| r_o \quad \text{ohms} \qquad [6\text{-}3]$$

If $r_o \geq 10\,R_C$

the approximation $R_C \| r_o \cong R_C$ is frequently applied and

$$Z_o \cong R_C \quad r_o \geq 10R_C \qquad [6\text{-}4]$$

A_v the resistor r_o and R_C are in parallel, and *But*

$$V_o = -\beta I_b (R_C \| r_o)$$

So that

$$V_o = -\beta \left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

And

$$A_v = \frac{V_o}{V_i} = \frac{(R_C \| r_o)}{r_e}$$

If $r_o \geq 10\,R_C$ *[6-5]*

$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C \qquad [6\text{-}6]$$

A_i

$$I_o = \frac{(r_o)(\beta I_b)}{r_o + R_C} \quad \text{and} \quad \frac{I_o}{I_b} = \frac{r_o \beta}{r_o + R_C}$$

With

$$I_b = \frac{(R_B)(I_i)}{R_B + \beta r_e} \quad \text{or} \quad \frac{I_b}{I_i} = \frac{R_B}{R_B + \beta r_e}$$

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_b}\right)\left(\frac{I_b}{I_i}\right) = \left(\frac{r_o \beta}{r_o + R_C}\right)\left(\frac{R_B}{R_B + \beta r_e}\right)$$

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} \qquad [6\text{-}7]$$

If $r_o \geq 10\,R_C$ and $R_B \geq 10\,\beta r_e$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_B r_o}{(r_o)(R_B)} \qquad A_i \cong \beta \quad r_o \geq 10R_C,\ R_B \geq 10\beta r_e \qquad [6\text{-}8]$$

For checking

$$A_i = -A_v \frac{Z_i}{R_C} \qquad [6\text{-}9]$$

***Phase Relationship**: the negative sign in the resulting equation for the A_v reveals that a 180º phase shift occurs between the input and output signals, as shown in fig6-5*

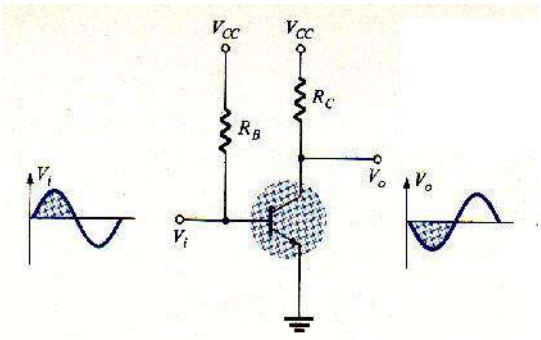


Fig6-5 180º phase shift between input & output

The simplicity of moving from one model to other by: $h_{fe} = \beta$ *and* $h_{ie} = \beta\, r_e$

Example 1: *For the network of Fig 6-6*

(a) Determine r_e.
(b) Find Z_i (with $r_o = \infty\ \Omega$).
(c) Calculate Z_o (with $r_o = \infty\ \Omega$).
(d) Determine A_v (with $r_o = \infty\ \Omega$).
(e) Find A_i (with $r_o = \infty\ \Omega$).
(f) Repeat parts (c) through (e) including $r_o = 50\ \text{k}\Omega$

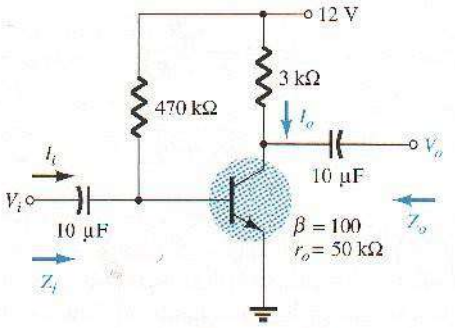


Fig 6-6

Solution:

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.069\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $$A_v = -\frac{R_C}{r_e} = -\frac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

(e) Since $R_B \geq 10\beta r_e (470\ \text{k}\Omega > 10.71\ \text{k}\Omega)$

$$A_i \cong \beta = \mathbf{100}$$

(f) ***Z_o***

$$= r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}\ \text{vs.}\ 3\ \text{k}\Omega$$

A_v

$$= -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = -264.24\ \text{vs.}\ -280.11$$

A_i

$$= \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 3\ \text{k}\Omega)(470\ \text{k}\Omega + 1.071\ \text{k}\Omega)}$$

$$= \mathbf{94.13}\ \text{vs.}\ 100$$

As a check ***A_i***

$$= -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ \text{k}\Omega)}{3\ \text{k}\Omega} = \mathbf{94.16}$$

2- Voltage Divider Bias (bypassed CE configuration)

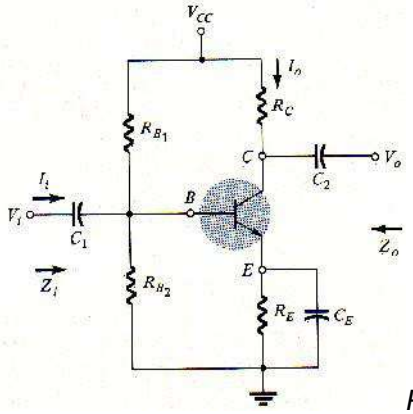


Fig6-7 voltage divider bias Configuration

Substituting the approximate r_e equivalent circuit will result the network of Fig7-8.

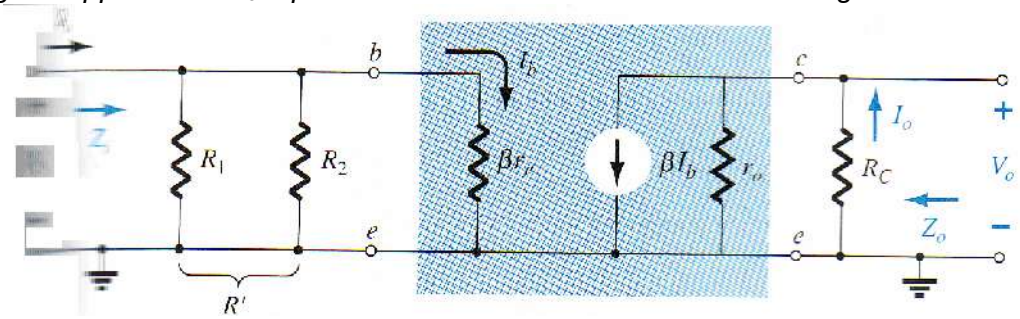


Fig6-8 substituting the r_e equivalent circuit into the ac equivalent network

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad [6\text{-}10]$$

Z_i

$$Z_i = R' \| \beta r_e \qquad [6\text{-}11]$$

Z_o with V_i = 0V resulting in I_b = 0 μA and βI_b = 0μA

$$Z_o = R_C \| r_o \qquad [6\text{-}12]$$

If $r_o \geq 10\,R_C$

$$Z_o \cong R_C \quad r_o \geq 10R_C \qquad [6\text{-}13]$$

A_v since R_C and r_o are in parallel

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and $$I_b = \frac{V_i}{\beta r_e}$$

so that $$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and $$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e} \qquad [6\text{-}14]$$

For $r_o \geq 10R_C$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \quad r_o \geq 10R_C \qquad [6\text{-}15]$$

A_i

$$A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)}$$ [6-16]

$$R' = R_1 \| R_2 = R_B,$$

For $r_o \geq 10\,R_C$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R' r_o}{r_o(R' + \beta r_e)}$$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R'}{R' + \beta r_e}, \quad r_o \geq 10R_C$$ [6-17]

$$A_i = \frac{I_o}{I_i} \cong \beta, \quad r_o \geq 10R_C,\ R' \geq 10\beta r_e$$ [6-18]

$$A_i = -A_v \frac{Z_i}{R_C}$$ [6-19]

For checking

***Phase Relationship**: the **negative sign** in the resulting equation for the A_v reveals that a 180º phase shift occurs between the output V_o and input V_i*

Example 2:

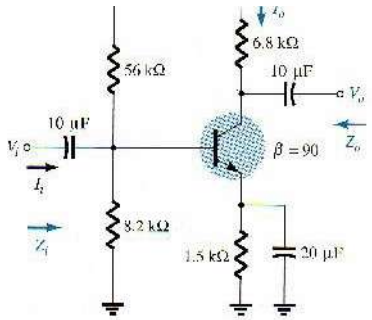


Fig6-9 Example 2

(a) Determine r_e.
(b) Find Z_i.
(c) Calculate Z_o (with $r_o = \infty\ \Omega$).
(d) Determine A_v (with $r_o = \infty\ \Omega$).
(e) Find A_i (with $r_o = \infty\ \Omega$).

(f) Find the parameters of parts (b) through (e) if $r_o = 1/h_{oe} = 50\ k\Omega$ and compare

Solution:

DC: Testing $\beta R_E > 10R_2$

$$(90)(1.5\ k\Omega) > 10(8.2\ k\Omega)$$
$$135\ k\Omega > 82\ k\Omega\ (satisfied)$$

The approximate approach:

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ k\Omega)(22\ V)}{56\ k\Omega + 8.2\ k\Omega} = 2.81\ V$$
$$V_E = V_B - V_{BE} = 2.81\ V - 0.7\ V = 2.11\ V$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\ V}{1.5\ k\Omega} = 1.41\ mA$$
$$r_e = \frac{26\ mV}{I_E} = \frac{26\ mV}{1.41\ mA} = \mathbf{18.44\ \Omega}$$

(b) $R' = R_1 \| R_2 = (56\ k\Omega) \| (8.2\ k\Omega) = 7.15\ k\Omega$
$Z_i = R' \| \beta r_e = 7.15\ k\Omega \| (90)(18.44\ \Omega) = 7.15\ k\Omega \| 1.66\ k\Omega$
$= \mathbf{1.35\ k\Omega}$

(c) $Z_o = R_C = \mathbf{6.8\ k\Omega}$

(d) $A_v = -\frac{R_C}{r_e} = -\frac{6.8\ k\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

(e) The condition $R' \geq 10\beta r_e$ (7.15 kΩ ≥ 10(1.66KΩ) = 16.6KΩ is not satisfied, Therefore

$$A_i \cong \frac{\beta R'}{R' + \beta r_e} = \frac{(90)(7.15\ \text{k}\Omega)}{7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega} = \mathbf{73.04}$$

(f) $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. 6.8 kΩ

$$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}\ \text{vs.}\ -368.76$$

The condition $r_o \geq 10R_C$ (50KΩ≥ 10(6.8KΩ) = 68KΩ) is not satisfied. Therefore

$$A_i = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)} = \frac{(90)(7.15\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 6.8\ \text{k}\Omega)(7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega)}$$
$$= \mathbf{64.3}\ \text{vs.}\ 73.04$$

3-CE Emitter-Bias Configuration a- Un bypassed

*Un bypassed configurations appears in Fig6-10. Substituting the approximate **r_e** equivalent model will result in Fig.6-11*

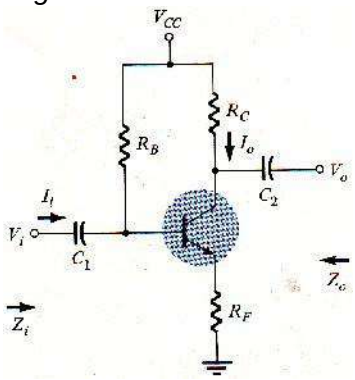


Fig6-10 CE Un bypassed configuration

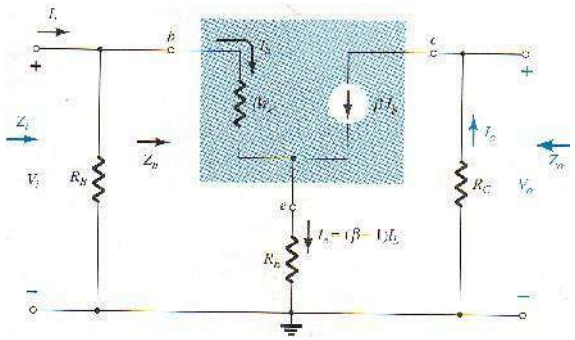


*Fig6-11 **r_e** equivalent for circuit of fig6-10*

$$V_i = I_b\beta r_e + I_e R_E$$

or

$$V_i = I_b\beta r_e + (\beta + 1)I_b R_E$$

and the input impedance looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \qquad [6\text{-}20]$$

β *Is normally* ***much greater than 1****, the approximate equation is the following*

$$Z_b \cong \beta r_e + \beta R_E$$

$$\boxed{Z_b \cong \beta(r_e + R_E)} \qquad [6\text{-}21]$$

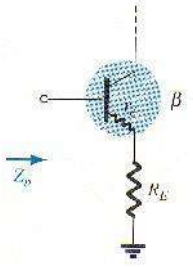


Fig6-12 the input impedance of an un bypassed CE

*Since R_E is often **much greater** than r_e*

$$Z_b \cong \beta R_E \qquad [6\text{-}22]$$

Z_i

$$Z_i = R_B \| Z_b \qquad [6\text{-}23]$$

Z_o *with* ***V_i*** *set to* ***zero,*** ***I_b*** *= 0 and* ***βI_b*** *can be replaced by an open - circuit*

$$Z_o = R_C \qquad [6\text{-}24]$$

A_v

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b} \qquad [6\text{-}25]$$

$Z_b = \beta(r_e + R_E)$ *gives*

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E} \qquad [6\text{-}26]$$

For the approximation ***$Z_b \approx \beta R_E$***

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E} \qquad [6\text{-}27]$$

A_i

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

$$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

In addition, $I_o = \beta I_b$

and $\frac{I_o}{I_b} = \beta$

so that $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\frac{I_b}{I_i}$

$$= \beta \frac{R_B}{R_B + Z_b}$$

and $$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{R_B + Z_b} \qquad [6\text{-}28]$$

or $$A_i = -A_v \frac{Z_i}{R_C} \qquad [6\text{-}29]$$

Phase Relationship*: the* ***negative sign*** *in the resulting equation for the* ***A_v*** *reveals that a 180º phase shift occurs between the output* ***V_o*** *and input* ***V_i***

Effect of r_o

Z_i

$$Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right]R_E$$

[6-30]

*Since the ratio R_C / r_o is always **much less** than (β + 1)*

$$Z_b \cong \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For $r_o \geq 10(R_C + R_E)$

$$Z_b \cong \beta r_e + (\beta + 1)R_E$$

*Since β+1 ≈ β the following equation is an **excellent one for most application**:*

[6-31]

$$Z_b \cong \beta(r_e + R_E) \qquad r_o \geq 10(R_C + R_E)$$

Z_o

[6-32]

$$Z_o = R_C \| \left[r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right]$$

However, $r_o >> r_e$ and

$$Z_o \cong R_C \| r_o \left[1 + \frac{\beta}{1 + \frac{\beta r_e}{R_E}} \right]$$

$$Z_o \cong R_C \| r_o \left[1 + \frac{1}{\frac{1}{\beta} + \frac{r_e}{R_E}} \right]$$

This can be written as

***1/β < 1**and **r_e/R_E <1 a sum usually less than one**. The result is a multiplying factor for **r_o greater than one**. For β=100, re =10Ω, and R_E =1kΩ:*

$$\frac{1}{\frac{1}{\beta} + \frac{r_e}{R_E}} = \frac{1}{\frac{1}{100} + \frac{10\ \Omega}{1000\ \Omega}} = \frac{1}{0.02} = 50$$

$Z_o = R_C \| 51 r_o$ *Which is certainly simply **R_C** . Therefore*

$$Z_o = R_C \qquad \text{Any level of } r_o$$

[6-33]

A_v

$$A_v = \frac{V_o}{V_i} = \frac{-\frac{\beta R_C}{Z_b}\left[1 + \frac{r_e}{r_o}\right] + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

[6-34]

$$\frac{r_e}{r_o} \ll 1$$

$$A_v = \frac{V_o}{V_i} \cong \frac{-\frac{\beta R_C}{Z_b} + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

$r_O \geq 10R_C$

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \qquad r_o \geq 10R_C$$

[6-35]

A_i

$$A_i = -A_v \frac{Z_i}{R_C}$$ *[6-36]*

---

b- Bypassed CE configuration

*If **R_E** of fig6-7 is bypassed by an emitter capacitor **C_E** the complete **r_e** equivalent model can be substituted resulting the same equivalent network as for fig 6-8*

***Example 3:** For the network of fig6-13, without C_E (un bypassed) determine:*

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

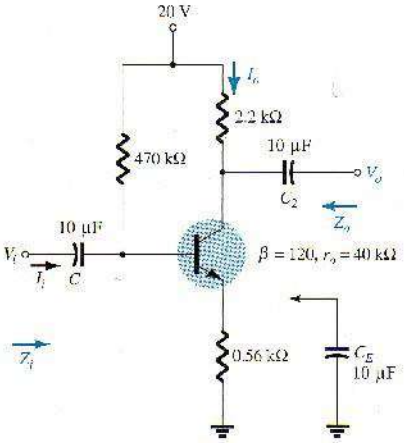


Fig6-13 Example 3:

Solution:

(a) DC: $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \dfrac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.8$

$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$

and $r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$

(b) Testing the condition $r_o \geq 10(R_C + R_E)$,

$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$

$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega$ *(satisfied)*

Therefore

$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$

$= 67.92\text{ k}\Omega$

and $Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega$

$= \mathbf{59.34\ k\Omega}$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

$r_o \geq 10R_C$** is satisfied. **Therefore

A_v

$$= \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\text{ k}\Omega)}{67.92\text{ k}\Omega}$$

$$= -3.89$$

*Compared to -3.93 using **$A_v \approx -R_C/R_E$***

A_i

$$= -A_v \frac{Z_i}{R_C} = -(-3.89)\left(\frac{59.34\text{ k}\Omega}{2.2\text{ k}\Omega}\right)$$

$$= 104.92$$

Compared to 104.85 using ***$A_i \approx \beta R_B / (R_B + Z_b)$***

Example 4: *Repeat the analysis of Example: 3 with C_E in place*

Solution:

(a) The dc analysis is the same, and $r_e = 5.99\ \Omega$.

(b) R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\ \text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\ \text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\ \text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28} \quad \text{(a significant increase)}$$

(e) $$A_i = \frac{\beta R_B}{R_B + Z_b} = \frac{(120)(470\ \text{k}\Omega)}{470\ \text{k}\Omega + 718.8\ \Omega}$$
$$= \mathbf{119.82}$$

Example 5: *For the network of fig6-14, determine (**using appropriate approximation**)*

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

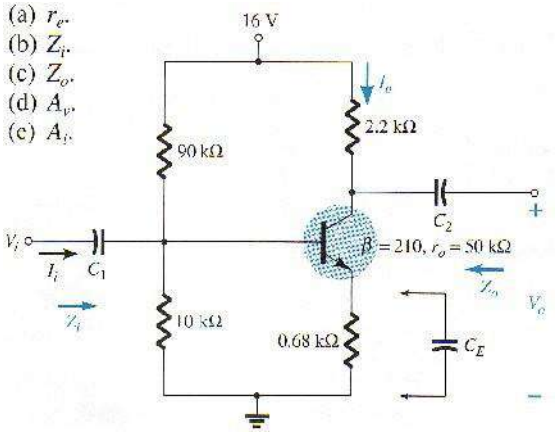


Fig6-14 Example5:

Solution:

$$\beta R_E > 10R_2$$
$$(210)(0.68\ \text{k}\Omega) > 10(10\ \text{k}\Omega)$$
$$142.8\ \text{k}\Omega > 100\ \text{k}\Omega\ (\textit{satisfied})$$
$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10\ \text{k}\Omega}{90\ \text{k}\Omega + 10\ \text{k}\Omega}(16\ \text{V}) = 1.6\ \text{V}$$
$$V_E = V_B - V_{BE} = 1.6\ \text{V} - 0.7\ \text{V} = 0.9\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{0.9\ \text{V}}{0.68\ \text{k}\Omega} = 1.324\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.324\ \text{mA}} = \mathbf{19.64\ \Omega}$$

(b) *The ac equivalent circuit is provided in fig6-15. The resulting configuration is now different from fig6-11 only by the fact that now*

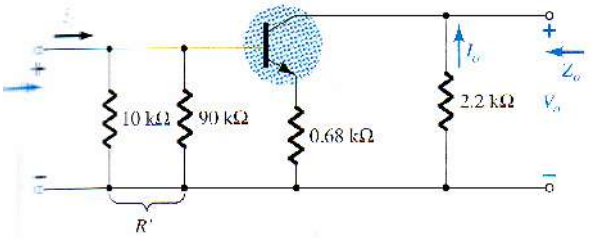


Fig6-15 ac equivalent

Testing condition of $\mathbf{r_o \geq 10(R_C + R_E)}$ and $\mathbf{r_o \geq 10R_C}$ are both satisfied. Using appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\ \text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 142.8\ \text{k}\Omega$$
$$= \mathbf{8.47\ k\Omega}$$

$$Z_o = R_C = \mathbf{2.2\ k\Omega}$$
$$A_v = -\frac{R_C}{R_E} = -\frac{2.2\ \text{k}\Omega}{0.68\ \text{k}\Omega} = \mathbf{-3.24}$$
$$A_i = -A_v \frac{Z_i}{R_C} = -(-3.24)\left(\frac{8.47\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$$
$$= \mathbf{12.47}$$

Repeat Example 5: with C_E in place

The dc analysis is the same, and $r_e = \mathbf{19.64\ \Omega}$.

$$Z_b = \beta r_e = (210)(19.64\ \Omega) \cong 4.12\ \text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 4.12\ \text{k}\Omega$$
$$= \mathbf{2.83\ k\Omega}$$
$$Z_o = R_C = \mathbf{2.2\ k\Omega}$$

(d) $$A_v = -\frac{R_C}{r_e} = -\frac{2.2\ \text{k}\Omega}{19.64\Omega} = -112.02 \text{ (a significant increase)}$$

(e) $$A_i = -A_v \frac{Z_i}{R_L} = -(-112.02)\left(\frac{2.83\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$$
$$= \mathbf{144.1}$$

4-Emitter-Follower Configuration

Since the output is taken from the emitter terminal of the transistor as shown in Fig6-16, the network is emitter-follower. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $\boldsymbol{A_v \approx 1}$. *The fact that* $\boldsymbol{V_o}$ *"follows" the magnitude of* V_i *with an in-phase relationship for the emitter-follower. The emitter-follower configuration used for impedance-matching purposes, it presents high impedance at the input and low impedance at the output*

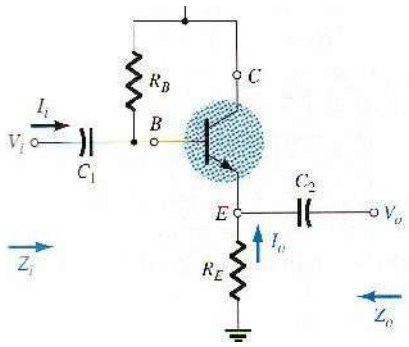


Fig 6-16 Emitter-follower configuration

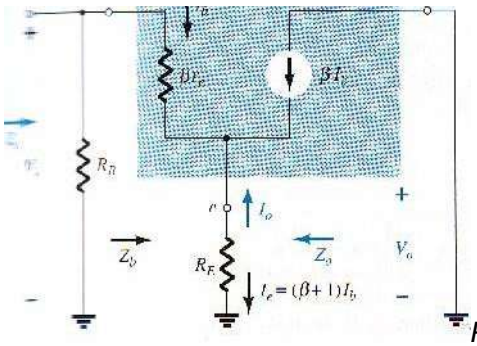


Fig6-17 ***re*** *model for network of fig 6-16*

Z_i

$$Z_i = R_B \| Z_b \qquad [6\text{-}37]$$

$$Z_b = \beta r_e + (\beta + 1)R_E \qquad [6\text{-}38]$$

$$Z_b \cong \beta(r_e + R_E) \qquad [6\text{-}39]$$

$$Z_b \cong \beta R_E \qquad [6\text{-}40]$$

Z_o

$$I_b = \frac{V_i}{Z_b}$$

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

but

$$(\beta + 1) \cong \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that

$$I_e \cong \frac{V_i}{r_e + R_E} \qquad [6\text{-}41]$$

Construct the network defined by the equation above; the configuration of fig 6-18 will result

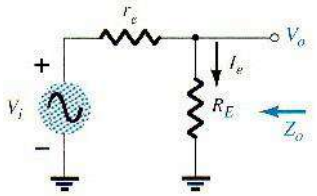


Fig6-18 the output impedance for Emitter-follower

*With **V_i** set to **zero***

$$Z_o = R_E \| r_e \qquad [6\text{-}42]$$

*Since R_E is typically much **greater** than r_e, the following approximation is*

$$Z_o \cong r_e \qquad [6\text{-}43]$$

A_v *the voltage divider rules*

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} \qquad [6\text{-}44]$$

*Since R_E is usually **much greater** than r_e, **$(R_E + r_e) \approx R_E$** and*

$$A_v = \frac{V_o}{V_i} \cong 1 \qquad [6\text{-}45]$$

A_i

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

or $$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

and $$I_o = -I_e = -(\beta + 1)I_b$$

or $$\frac{I_o}{I_b} = -(\beta + 1)$$

so that $$A_i = \frac{I_o}{I_i} = \frac{I_o I_b}{I_b I_i} = -(\beta + 1)\frac{R_B}{R_B + Z_b}$$ *[6-46]*

and since $(\beta + 1) \cong \beta$,

$$A_i \cong -\frac{\beta R_B}{R_B + Z_b}$$

or

$$A_i = -A_v \frac{Z_i}{R_E}$$ *[6-47]*

***Phase Relationship**: the resulting equation for the A_v reveals that the output **V_o** and input **V_i** are in phase for the emitter-follower configuration*

Effect of r_0 Z_i

$$Z_b = \beta r_e + \frac{(\beta - 1)R_E}{1 + \frac{R_L}{r_o}}$$ *[6-48]*

$R_o \geq 10R_E$ is satisfied

$$Z_b = \beta r_e + (\beta + 1)R_E$$

$$Z_b \cong \beta(r_e + R_E)$$ *$r_o \geq 10R_E$* *[6-49]*

Z_o

$$Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)}$$ *[6-50]*

$$Z_o = r_o \| R_E \| r_e$$

$r_o >> r_e$

$$Z_o \cong R_E \| r_e$$ Any r_o *[6-51]*

A_v

$$A_v = \frac{(\beta + 1)R_L / Z_b}{1 + \frac{R_L}{r_o}}$$ *[6-52]*

$R_o \geq 10R_E$ is satisfied** and we use the approximation **$\beta + 1 \approx \beta$

$$A_v \cong \frac{\beta R_E}{Z_b}$$

$$Z_b \cong \beta(r_e + R_E)$$

$$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

$$\boxed{A_v \cong \frac{R_E}{r_e + R_E}} \quad r_o \geq 10R_E \qquad [6\text{-}53]$$

Example 7: *For the emitter-follower network of Fig6-19 determine;*

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

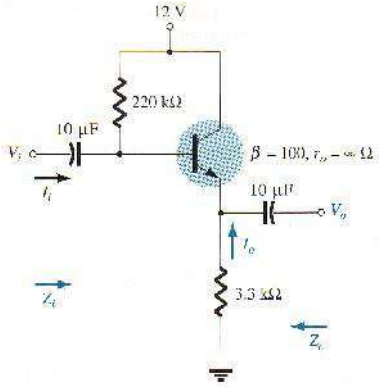


Fig6-19 example 7:

Repeat part (b) through (e) with r_o = 25KΩ and compare result

Solution:

(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)3.3\text{ k}\Omega} = 20.42\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B$$

$$= (101)(20.42\ \mu\text{A}) = 2.062\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = \mathbf{12.61\ \Omega}$$

(b) $$Z_b = \beta r_e + (\beta + 1)R_E$$

$$= (100)(12.61\ \Omega) + (101)(3.3\text{ k}\Omega)$$

$$= 1.261\text{ k}\Omega + 333.3\text{ k}\Omega$$

$$= 334.56\text{ k}\Omega \cong \beta R_E$$

$$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 334.56\text{ k}\Omega$$

$$= \mathbf{132.72\ k\Omega}$$

(c) $$Z_o = R_E \| r_e = 3.3\text{ k}\Omega \| 12.61\ \Omega$$

$$= \mathbf{12.56\ \Omega} \cong r_e$$

(d) $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\text{ k}\Omega}{3.3\text{ k}\Omega + 12.61\ \Omega}$$

$$= \mathbf{0.996} \cong \mathbf{1}$$

(e) $$A_i \cong -\frac{\beta R_B}{R_B + Z_b} = -\frac{(100)(220\ \text{k}\Omega)}{220\ \text{k}\Omega + 334.56\ \text{k}\Omega} = \mathbf{-39.67}$$

versus

$$A_i = -A_v\frac{Z_i}{R_E} = -(0.996)\left(\frac{132.72\ \text{k}\Omega}{3.3\ \text{k}\Omega}\right) = \mathbf{-40.06}$$

(f) Checking the condition $r_o \geq 10R_E$, we have

$$25\ \text{k}\Omega \geq 10(3.3\ \text{k}\Omega) = 33\ \text{k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\ \text{k}\Omega}{1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}}$$

$$= 1.261\ \text{k}\Omega + 294.43\ \text{k}\Omega$$

$$= 295.7\ \text{k}\Omega$$

$$Z_i = R_B \| Z_b = 220\ \text{k}\Omega \| 295.7\ \text{k}\Omega$$

$$= \mathbf{126.15\ k\Omega}\ \text{vs.}\ 132.72\ \text{k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \dfrac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\ \text{k}\Omega)/295.7\ \text{k}\Omega}{\left[1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}\right]}$$

$$= \mathbf{0.996} \cong 1$$

Matching the earlier result

Therefore, a good approximation for the actual results can be obtained by simply ignoring the effects of r_o for this configuration.

The network of fig6-20 equations changed only by replacing $\mathbf{R_B}$ by $\mathbf{R'} = \mathbf{R_1} \parallel \mathbf{R_2}$

Fig6-21 will also provide the input/output characteristics of an emitter-follower but includes a collector resistor $\mathbf{R_C}$.
In this case $\mathbf{R_B}$ is again replaced by the parallel combination of $\mathbf{R_1}$ and $\mathbf{R_2}$. The input impedance $\mathbf{Z_i}$ and output impedance $\mathbf{Z_o}$ are unaffected by $\mathbf{R_C}$ since it is not ret1ected into the base or emitter equivalent. In fact, the only effect of $\mathbf{R_C}$ will be to determine the **Q-point** of operation

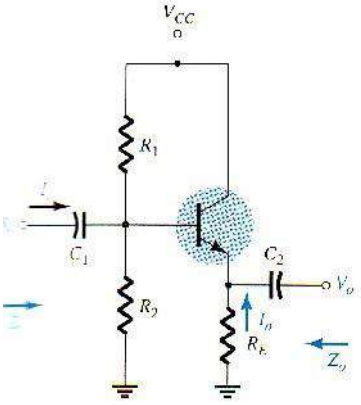


Fig6-20E-follower with voltage divider

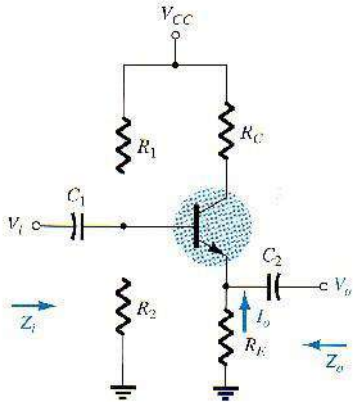
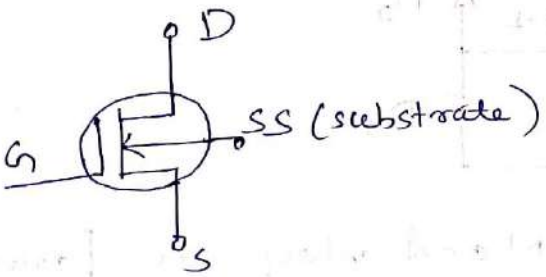


Fig6-21 E-follower with R_C

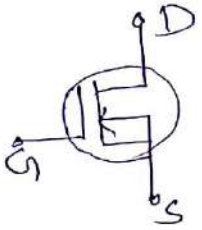
MOSFET:

Depletion type MOSFET symbol

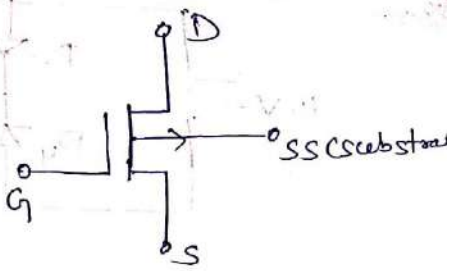
n channel



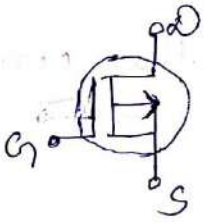
⇓ can be drawn



P channel

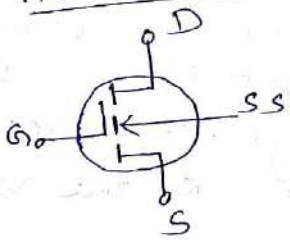


⇓ can be drawn

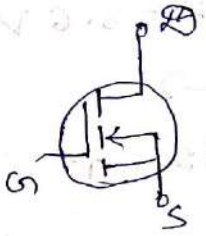


Enhancement type MOSFET symbol (Dashed line)

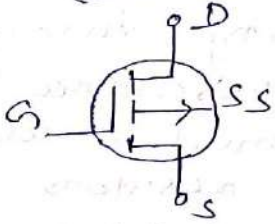
n channel



⇓



P channel



⇓

DMOSFET

i) Channel is available initially.

ii) Diffused channel

iii) Operates or can be operated in both Depletion & enhancement mode.

iv) Can be designed in Self biased arrangement.

v) Comparatively larger in size and expensive

vi) When $V_{GS}=0$, $I_D=I_{DSS}$

vii) No channel length modulation

EMOSFET

i) Channel is not present initially.

ii) Induced Channel

iii) Suitable for only Enhancement mode.

iv) Can't be designed in selfbiased arrangement.

v) Comparatively smaller in size, and economical for use.

vi) When $V_{GS}=0$, $I_D=0$

vii) Channel length modulation is there

MOSFET

(Metal Oxide Field Effect Transistor)

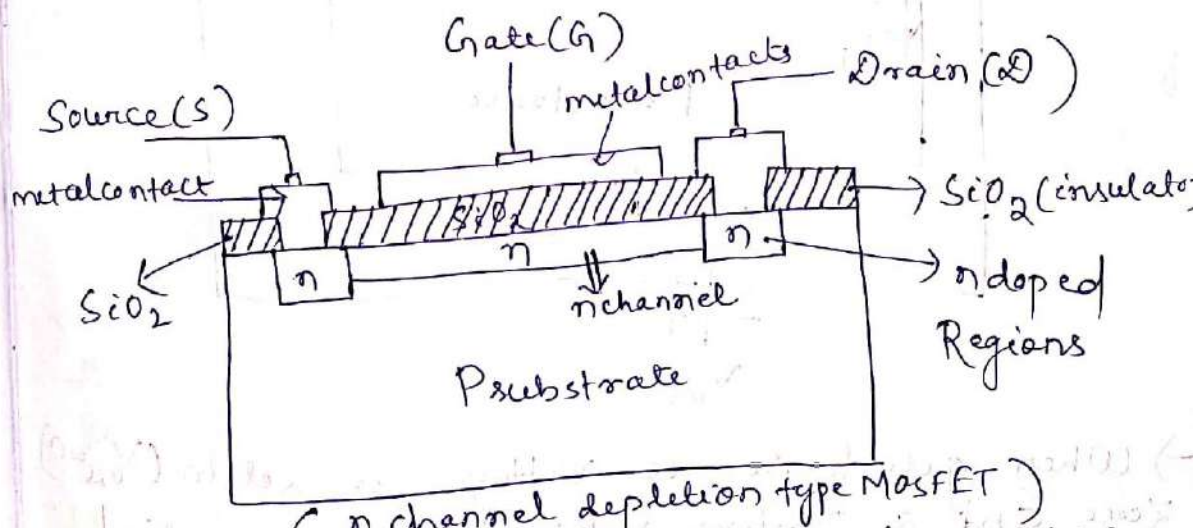
Mosfet has high input impedance and low cost of production as compared to JFET.

Types of MOSFET :—

1. Depletion-type MOSFET or DMOSFET → This mosfet can be operated in both Depletion mode & enhancement mode.
2. Enhancement-type MOSFET or EMOSFET → It can only be operated in enhancement mode.

→ MOSFET has four terminals :—
(i) Drain (ii) Gate (iii) Source (iv) Body or Substrate

DEPLETION TYPE MOSFET :— (n channel)



(n channel depletion type MOSFET)

→ P type material is present as base which is referred to as substrate.
→ On some cases substrate is internally connected to the source terminal.
→ The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel.

→ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

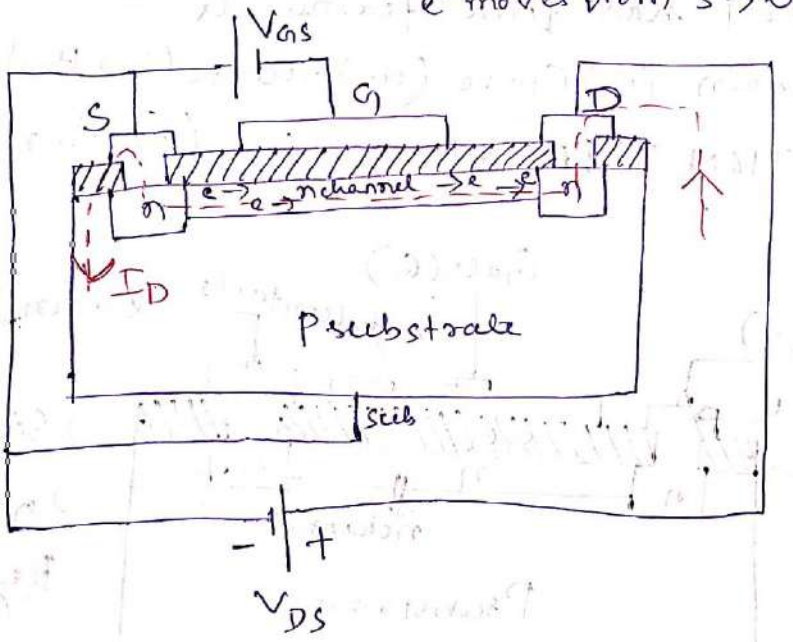
→ SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field.

Basic Operation

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

I_D = Drain current (flows from D → S)
e⁻ moves from S → D



→ When gate-to-source voltage is set to ($V_{GS}=0$) zero and a positive voltage $V_{DS}>0$ is applied, then as drain is at more potential as compared to source, so, the result is an attraction for the positive potential at the drain by free electrons of the n channel.

→ When V_{GS} is set at negative voltage ($V_{GS} < 0V$) then the negative potential at the gate will tend to prescere electrons towards the p-type substrate and will attract holes from the p-type substrate.

→ Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occcur that will reduce the number of free electrons in the n-channel available for conduction.

→ The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

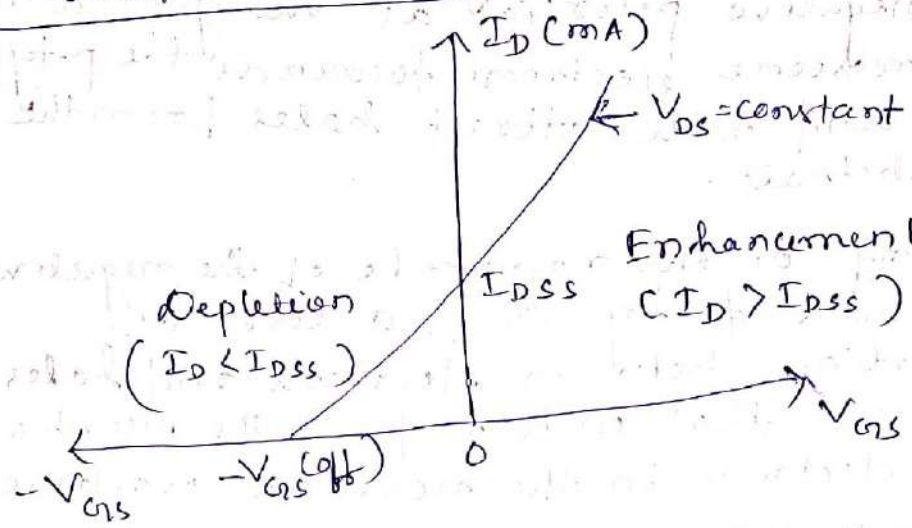
* For positive values of V_{GS}, the positive gate will draw additional electrons from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.

→ With the V_{GS} increment in positive direction, the drain current will increase in rapid rate.

→ The positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to $V_{GS} = 0V$.

→ For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region, with the region between cutoff and saturation level of I_{DSS} referred to as the depletion region.

DMOSFET Characteristics :- (n channel)



(I_D Vs V_{GS}) ⇒ Transfer characteristic

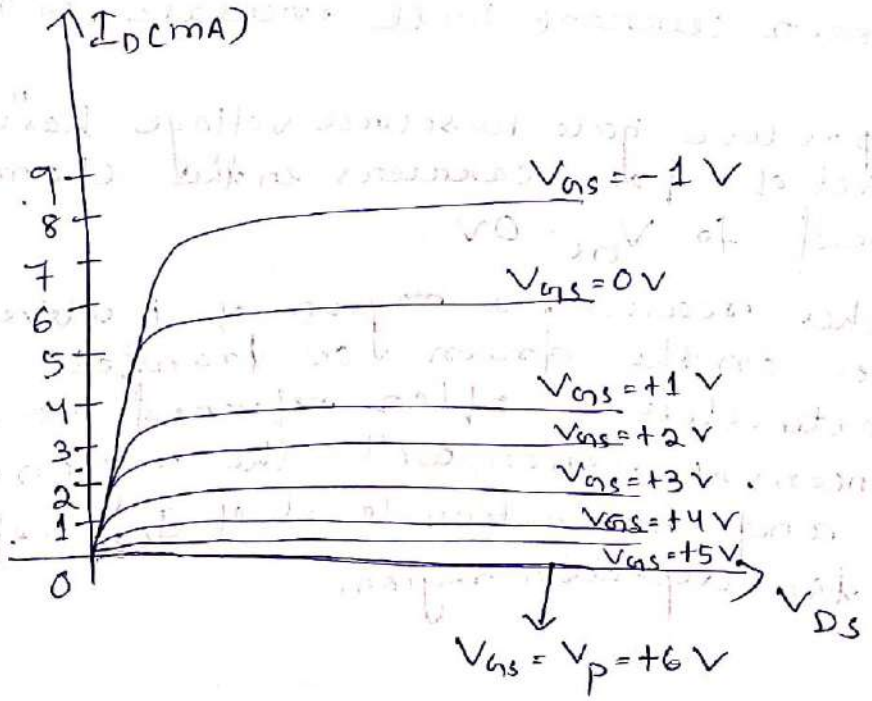
I_{DSS} is present when $V_{GS} = 0$ V

I_{DSS} = drain to source current with gate shorted ($V_{GS} = 0$)

I_D = Drain current

Characteristics :- (n channel)

I_D Vs V_{DS} when V_{GS} is applied :-



Shockley's equation for D-MOSFET:-

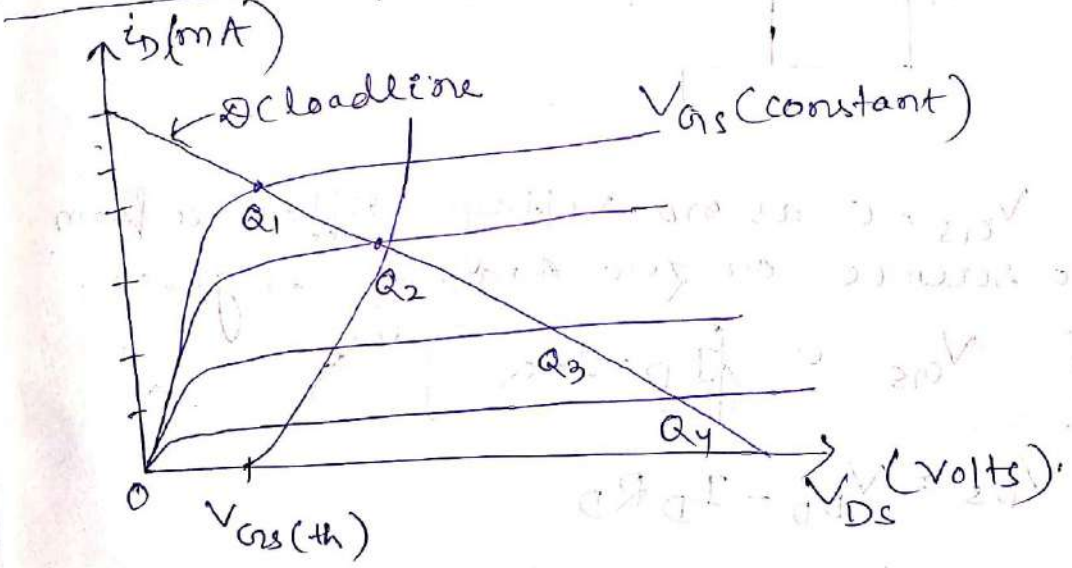
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

V_P = pinchoff voltage

Pinchoff refers to the threshold voltage below which the transistor turns off.

*. To get the Q point we have to get V_{GSQ} & I_{DQ} of MOSFET.

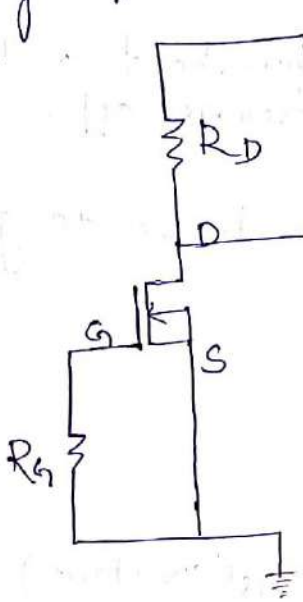
DC loadline & Q point



Biasing of ⊗ MOSFET :-

(i) Zero biasing (ii) Self biasing (iii) Voltage Divider

Zero biasing of n channel ⊗ MOSFET :-



Here $V_{GS} = 0$ as no voltage difference from gate to source or zero biasing is given.

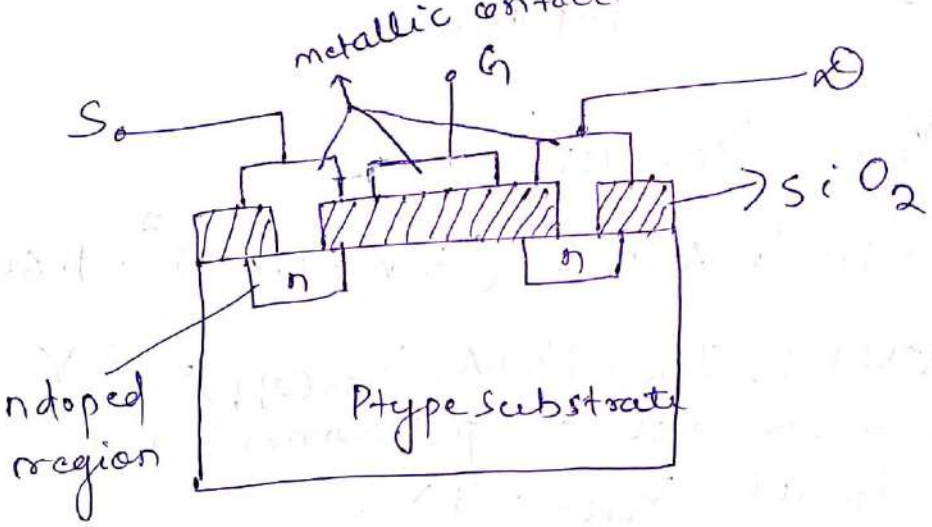
So $V_{GS} = 0$ $\Rightarrow$ $\boxed{I_D = I_{DSS}}$ &

$$V_{DS} = V_{DD} - I_D R_D$$

V_{DS} can be measured w.r.t source as source terminal is grounded.

*. Since ⊗ MOSFET can be operated with either positive or negative values of V_{GS}, we can set its Qpoint at $V_{GS} = 0$ V.

n channel Enhancement MOSFET :—
(no channel initially)



ENHANCEMENT-TYPE MOSFET (N Channel)

→ The construction of EMOSFET is similar to that of DMOSFET but here no channel (n type) is not present initially in between two n-doped regions. (For construction refer to DMOSFET and here no channel is present initially)

→ The SiO_2 layer is present to isolate the gate metallic platform from the region between the drain and source.

Operation:-

→ If $V_{GS} = 0V$ and a voltage is applied between the drain and source of the device due to the absence of an n channel (absence of free carriers in between drain & source) and it will result in no current from D → S but we are getting $I_D = I_{DSS}$ when $V_{GS} = 0V$ in case of DMOSFET as channel is initially present.

→ With $V_{DS}, V_{GS} > 0V$, establishing the drain and gate at a positive potential w.r.t. the source.

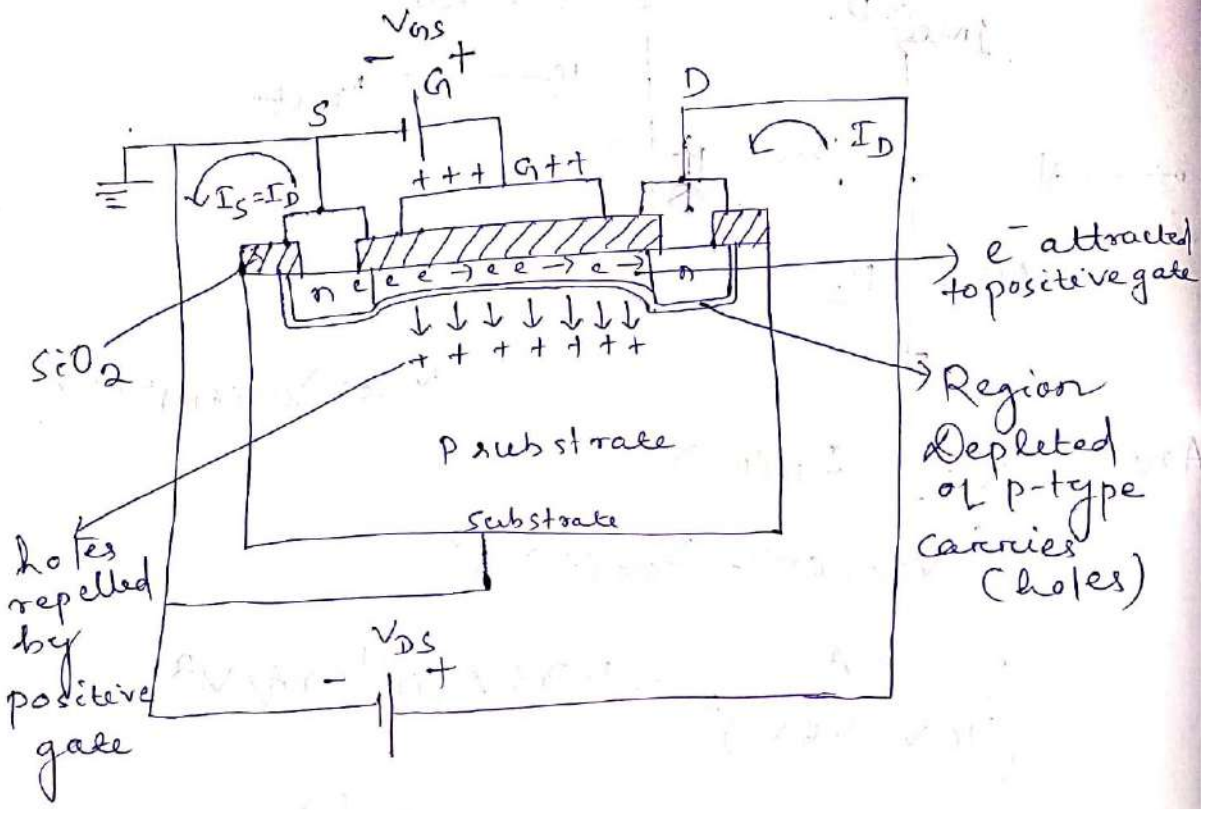
→ The positive potential at the gate will pressure the holes in the p substrate along the edge of SiO_2 layer to leave the area and enter deeper regions of 'p' substrate.

⇒ The result is a depletion region near the SiO_2 insulating layer void of holes. The e^- in the p-substrate (minority carriers) will be attracted to the positive gate and accumulate in the region near the surface of SiO_2 layer.

→ The SiO_2 insulating layer will prevent the negative carriers from being absorbed at the gate terminal.

→ As V_{GS} increases in magnitude, the concentration of e^- near the SiO_2 surface increases until the induced n-type region can support a measurable flow between drain & source.

Enhancement n channel MOSFET with V_{GS} & V_{DS}:-



→ The level of V_{GS} that results in significant increase in drain current is called as 'THRESHOLD VOLTAGE' and symbol is V_T.

→ At $V_{GS} = 0V$ no channel is present and channel is enhanced by $V_{GS} > 0V$, so this is called as ENHANCEMENT-type MOSFET.

→ If we hold V_{GS} constant and increase the level of V_{DS}, drain current will reach a saturation level

→ $\boxed{V_{DG} = V_{DS} - V_{GS}}$ (as source is connected to -ve)

→ If V_{DS} is increased and V_{GS} is held constant then V_{DG} also increases that means drain is at more potential w.r.t gate.

→ The saturation value of V_{DS} is related to V_{GS} by:

$$\boxed{V_{DS(sat)} = V_{GS} - V_T}$$

→ So current (I_D) increases when $V_{GS} > V_T$ so,

$$\boxed{I_D = k(V_{GS} - V_T)^2} \quad \text{-Imp.}$$

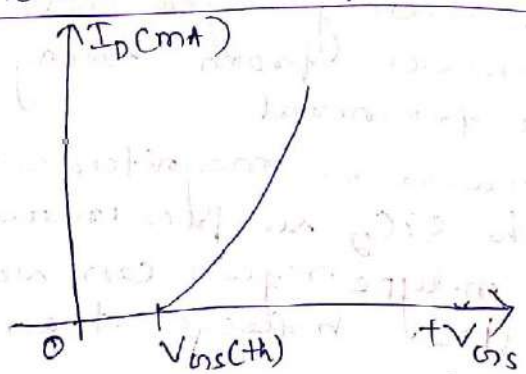
k = constant that is a function of construction of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

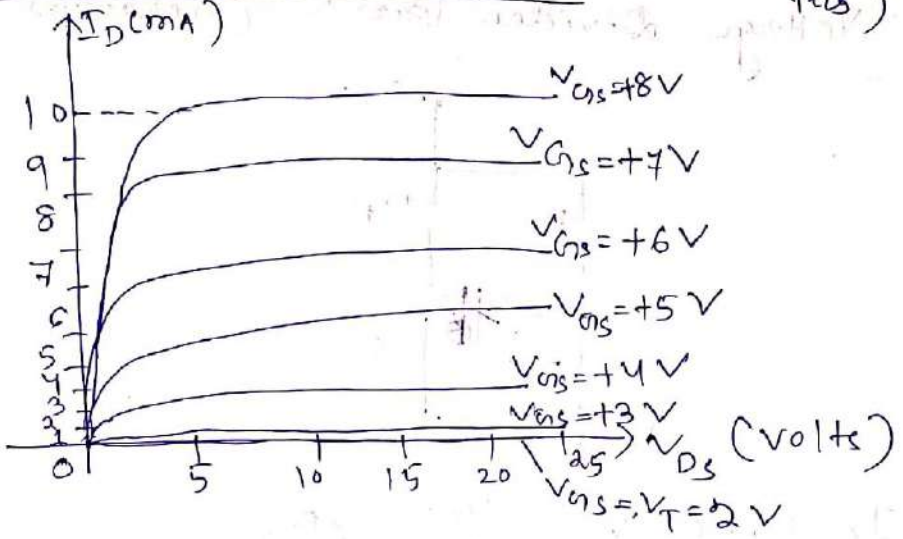
*. So here I_D & V_{GS} are in nonlinear relationship

EMOSFET n channel transfer characteristics:-

I_D Vs V_{GS} :-



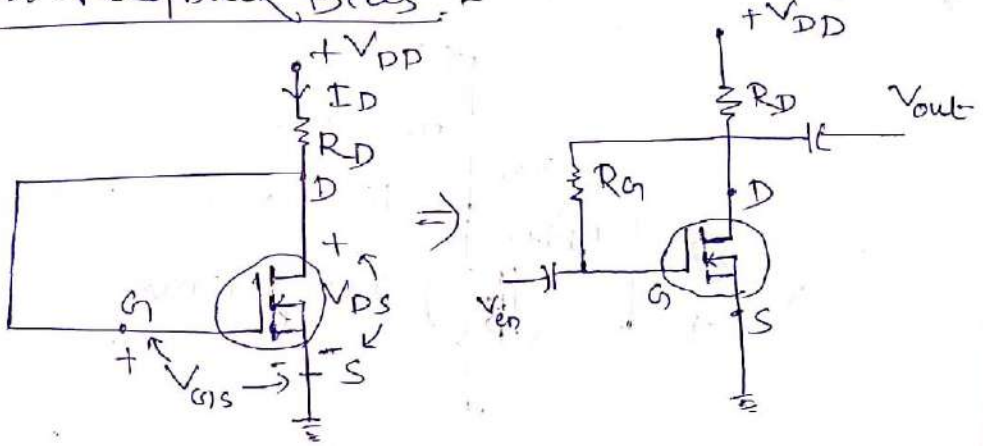
I_D Vs V_{DS} (n channel EMOSFET) (Drain characteristics)



EMOSFET Biasing :-

As $\boxed{V_{GS} > V_T}$ to turn on so zero bias or $V_{GS}=0$ can't be used.

(i) Drain-Feedback Bias :-



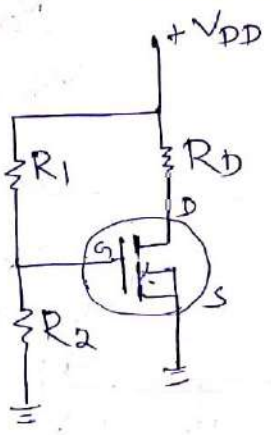
Two figures show this biasing technique. As for n channel EMOSFET, A high resistance R_G is connected between the drain & gate ($\because I_G=0$), therefore, voltage drop accross R_G=0V and the gate will be at same potential as the drain.

$$V_D = V_G \quad \text{and} \quad V_{DS} = V_{GS}$$

So $\boxed{V_{DS} = V_{DD} - I_D R_D = V_{GS}}$, $I_D = I_{D(on)}$

-) So V_{GSQ}, I_{DQ} are obtained to get Q point.
-) This is similar to collector-feedback biasing in BJT.

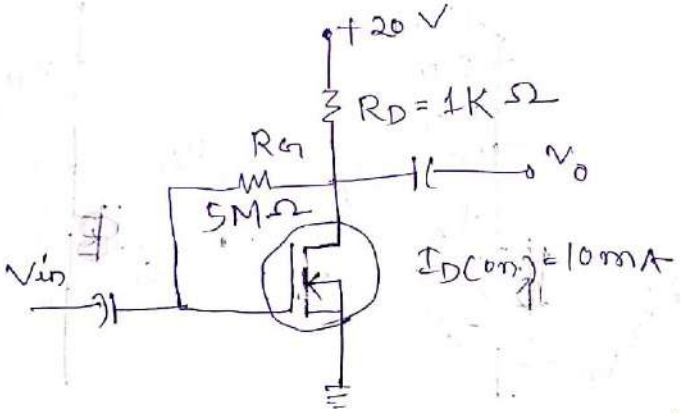
(ii) Voltage Divider Bias :— (n-channel EMOSFET)



$I_G = 0$, so $V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$

$\boxed{V_{DS} = V_{DD} - I_D R_D}$ where $I_D = K(V_{GS} - V_{GS(th)})^2$

* Determine I_D & V_{DS} :— $I_{D(on)} = 10\,mA$ (given)



Ans- $V_{GS} = V_{DS}$ (as source is grounded and R_G is in MΩ so $I_G = 0$)

$R_D = 1K\Omega$ (given), $V_{DD} = +20V$ (given), $R_G = 5M\Omega$ (given)

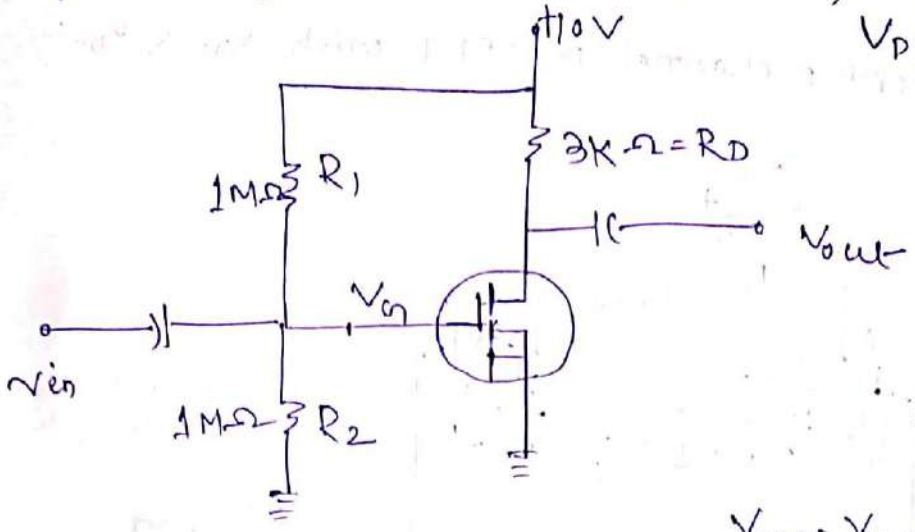
$V_{DS} = V_{DD} - I_D R_D = 20V - 10mA \times 1K\Omega$

$= 20 - 10 = 10V$

This is EMOSFET Drain feedback biasing.

Q. Determine the value of I_D.

Given:- $I_{D(on)} = 10\,mA$, $V_{GS} = 10\,V$, $V_{GS(th)} = 1.5\,V$



$V_{GS} = V_{GS(on)} = 10\,V$

Ans:- $K = \dfrac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$

$= \dfrac{10\,mA}{(10\,V - 1.5\,V)^2} = 1.38 \times 10^{-1}\,mA/V^2$

$V_S = 0$ (as source is grounded)

So $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_{GS(on)}$

$V_G = \dfrac{V_{DD}}{R_1 + R_2} \times R_2 = \dfrac{10\,V}{(1+1)M\Omega} \times 1M\Omega = 5\,V$

$I_D = K(V_{GS} - V_{GS(th)})^2$

$= (1.38 \times 10^{-1}\,mA/V^2)(5\,V - 1.5)^2 = 1.69\,mA$

Q. For a D MOSFET, $I_{DSS} = 10\,mA$, $V_{GS(off)} = -8\,V$.

(a) Is this an n-channel or p-channel?

(b) Calculate I_D at $V_{GS} = -3\,V$.

(c) Calculate I_D at $V_{GS} = +3\,V$.

Ans-(a) As $V_{GS(off)}$ is -ve so it is n-channel MOSFET.

(b) $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2 = 10\,mA\left(1 - \left(\dfrac{-3\,V}{-8\,V}\right)\right)^2$

$= 3.91\,mA$

(c) $I_D = 10\,mA \times \left(1 - \left(\dfrac{+3\,V}{-8\,V}\right)^2\right)^2 = 18.9\,mA$

MODULE III

DIGITAL ELECTRONIC PRINCIPLES:

We know there are two types of signals, one is analog or continuous signal and the second one is Digital or discrete signal. So the science or field of research in the area of engineering is termed as Analog and **Digital Electronics** respectively. Now coming to the area of Digital Electronics, it is essential to understand wide range of applications from industrial electronics to the fields of communication, from micro embedded systems to military equipment. The main and perhaps the most revolutionary **advantage of digital electronics** is the decrease in size and the improvement in technology.

Advantages of digital signal

- Carry more information per second than analogue signals
- Maintain quality over long distances better than analogue signals.
- They're automatic
- Easier to remove noise
- Can be very immune to noise

Binary Digit and Logic Levels

There are two digits in binary system. 0 and 1 called bits. Bit is contraction of two words **Bi**nary Digi**t**.

Digital Waveforms

Digital waveform are voltages levels changing back and forth between HIGH and LOW levels or states.Usually these waveforms are represented as timing diagrams used to represent wave behavior relative to time,

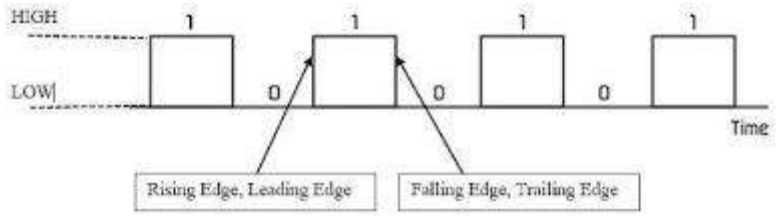


Figure 2

Pulse indicated in Figure 2 has two edges: A leading edge where pulse goes to HIGH from LOW state and Falling edge where pulse revert. However it is non ideal pulse representation because sudden transition from one state to other is impractical. Depending on practical consideration it will take small amount of time to get HIGH transition from LOW and vice versa,

Rise Time: ***Time required for pulse to go from its LOW level to HIGH is called rise time*** **tr.**

Fall Time: ***Time required for pulse to go from its HIGH level to LOW level is called fall time*** **tf.**

Pulse Width: ***It is measure of duration between rise edge and fall edge of the pulse indicated as*** **tw.**

Frequency (*f) and Time Period T:*

Frequency of a periodic (which repeats itself) waveform is the rate at which it repeats itself and measured in *Hz.* Whereas time period is duration after that signal or waveform repeats itself. Mathematical interpretations are given below in equation *(i)* and *(ii)* .

$$f = 1/T \ \ \textbf{Hz} \qquad (i)$$

$$T = 1/f \ \ \textbf{s} \qquad (ii)$$

Duty Cycles

A more essential characteristic of a periodic signal that is ratio of pulse width to the time period.

$$\text{Duty Cycle} = (\text{Pulse-width} / T)\ 100\%$$

1. Decimal Number System

The number system that we use in our day-to-day life is the decimal number system. Decimal number system has base 10 as it uses 10 digits from 0 to 9. In decimal number system, the successive positions to the left of the decimal point represents units, tens, hundreds, thousands and so on.

Each position represents a specific power of the base (10). For example, the decimal number 1234 consists of the digit 4 in the units position, 3 in the tens position, 2 in the hundreds position, and 1 in the thousands position, and its value can be written as

2.	**Binary Number System** Base 2. Digits used: 0, 1
3	**Octal Number System** Base 8. Digits used: 0 to 7
4	**Hexa Decimal Number System** Base 16. Digits used: 0 to 9, Letters used: A- F

Binary to Decimal Conversion

Conversion of Integer Numbers

Just as you can convert any binary numbers to hexadecimal, or convert binary numbers to octal, any number in the binary number system can be converted into the hexadecimal number system.
This conversion is also very simple method. Let, a binary number be $(11010)_2$, where the weight of the binary digits from most significant bit are 2^4, 2^3, 2^2, 2^1, 2^0 respectively.

Now the bits are multiplied with their weights, and the sum of those products is the respective decimal number. Now let us follow the following steps mathematically:

$$(11010)_2 \rightarrow 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$$
$$= 16 + 8 + 2 = (26)_{10}$$
$$\therefore (11010)_2 = (26)_{10}$$

Hence, $(26)_{10}$ is the required decimal number. This is how binary to decimal conversion is performed.
As another example, we convert the binary number $(1110)_2$ to a decimal number:

$$(1110)_2 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = (15)_{10}$$

Convert Binary Number to Decimal Number

Conversion of Decimal Point Number to Decimal

This can also be done in the same way, however after the decimal point the number should be multiplied with 2^{-1}, 2^{-2} etc.
For example,

$$(1110.011)_2 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$
$$= (15.375)_{10}$$

Decimal to Binary Conversion

Integer Decimal Numbers to Binary

Divide the number by 2 and take only the remainder, if division is completed than take only the remainder which gives the binary number. Suppose we are converting the decimal number $(87)^{10}$. We divide 87 by 2 and get 43 as the quotient and 1 as the remainder. These remainders are written beside as shown below.

2	87	→	1
2	43	→	1
2	21	→	1
2	10	→	0
2	5	→	1
2	2	→	0
	1		

The possibility of remainder $(87)_{10} = (1010111)_2$ is only 1 and 0. Thus the number is counted from the last remainder. Such as 1 → 0 → 1 → 0 → 1 → 1 → 1. This is how **decimal to binary conversion** is done.

Fraction Decimal Numbers to Binary

In this case, the successive multiplication is done. The number which is to be converted is multiplied with base or radix of binary number which is 2. The integer part or the carry of the product is taken out and the same process is repeated until we get an integer. For example-The binary equivalent of $(.95)_{10}$ is evaluated as follows-

$$.95 \times 2 = 1.90 - - - - - - - - - - 1 \; is\ taken\ out$$
$$.90 \times 2 = 1.80 - - - - - - - - - - 1$$
$$.80 \times 2 = 1.60 - - - - - - - - - - 1$$
$$.60 \times 2 = 1.20 - - - - - - - - - - -1$$
$$.20 \times 2 = .40 - - - - - - - - - - - - -1$$
$$.40 \times 2 = .80 - - - - - - - - - - - - -0$$

Since, we are not getting the integer value after successive multiplication, we can approximate the value to be $(.111110\ldots)_2$.

Negative Decimal to Binary

In case of a negative number we can go for 2's complement representation of a signed number.
Example- 9 = 0000 1001
1's complement = 1111 0110.
Adding 1 we get = 11110111 which is the 2's complement representation of (-9).

Binary representation of 5 is: 0 1 0 1

1's Complement of 5 is: 1 0 1 0

2's Complement of 5 is: (1's Complement + 1) i.e.

1 0 1 0 (1's Compliment)

\+ 1

1 0 1 1 (2's Complement i.e. -5)

BINARY ARITHMETIC

The **arithmetic of binary numbers** means the operation of addition, subtraction, multiplication and division. **Binary arithmetic** operation starts from the least significant bit i.e. from the right most side.

Binary Addition

There are four steps in binary addition, they are written below

- 0 + 0 = 0
- 0 + 1 = 1
- 1 + 0 = 1
- 1 + 1 = 0 (carry 1 to the next significant bit)

An example will help us to understand the addition process. Let us take two binary numbers 10001001 and 10010101

```
        1
   10001001
   10010101
-----------
  100111110
```

The above example of **binary arithmetic** clearly explains the binary addition operation, the carried 1 is shown on the upper side of the operands.

Binary Subtraction

Here are too four simple steps to keep in memory

- 0 – 0 = 0
- 0 – 1 = 1, borrow 1 from the next more significant bit
- 1 – 0 = 1
- 1 – 1 = 0

Suppose, A = 10101100 and B = 1010100 and we want to find out A – B.

Now implementing the rules of binary subtraction

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
              0
```

The first step is 0 – 0 = 0 and that's what is written in the place for result

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
            0 0
```

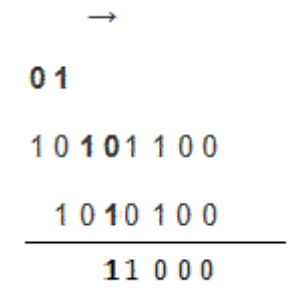
Similarly again the last step is repeated as here the numbers are both 0 and from the table we know 0 – 0 = 0.

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
          0 0 0
```

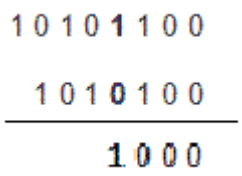
From the table we can find out that 1 – 1 = 0 and it is written

```
1 0 1 0 1 1 0 0
  1 0 1 0 1 0 0
-----------------
        1 0 0 0
```

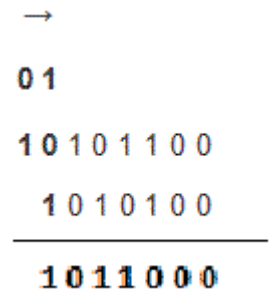
The table shows that 1 – 0 = 1 and we have written exactly that in result



Here 0 – 1 = 1 with borrowing of 1 from the next significant bit and that's what has been done. We will treat the next 1 as 0 in the next step as shown below.



As the 1 was borrowed in the previous step we are treating the 1 as 0 and the result is 0 – 0 = 0 and that is written



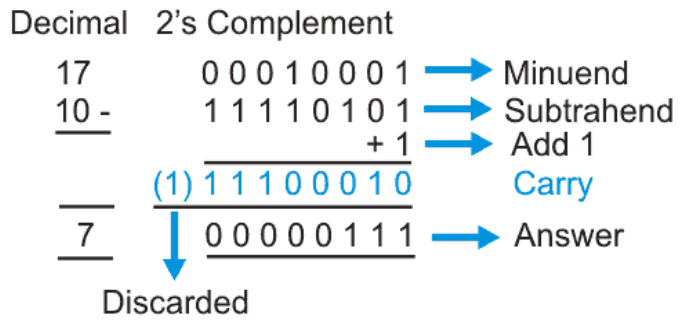
Again the last 1 has been borrowed because the operation done was 0 – 1 = 1 with borrow 1 from the next most significant bit and the final result of **binary subtraction**, we got is written in the place of result in the final step.

Why We Do Need 2's Complement?

The main problem of using **2's complement** is that it can be used for subtraction for two binary digits. The computer understands only binary as we know, and there is nothing called as negative number in the binary number system but it is absolutely necessary to represent a negative number using binary which can be done by assigning a sign bit to the number which is an extra bit required. If the sign bit is 1 then number is considered negative and if it is 0, than it will be the number will be called as positive.
For subtraction of binary numbers that can be done as follows-

Subtracting a Smaller Number from a Larger Number

1. **Find 2's complement of the smaller number.**
2. **Add the larger and 2's complement of the smaller number.**
3. **Discard the carry.**
4. **After discarding the carry, keep the result which will be answer for subtraction.**



Subtracting Larger Number from Smaller Number

1. Find 2's complement of larger number.
2. Add 2's complement of larger number to the smaller number.
3. If no carry is generated, find the 2's complement of the result and the result will be negative.
4. If carry is generated, discard the carry and take the result which will be the answer and the sign will be negative.

+ 75 0 1 0 0 1 0 1 1
- 75 1 0 1 1 0 1 0 1 (2's Complement form)

+ 26 0 0 0 1 1 0 1 0
- 75 1 0 1 1 0 1 0 1 (2's Complement form of - 75)
- 49 1 1 0 0 1 1 1 1 (No Carry)

Subtraction of larger number from smaller number.

Binary Multiplication

Like in case of binary addition and **binary multiplication** there are also four steps to be followed during a bigger multiplication or we can say these fundamental steps as well.
These are

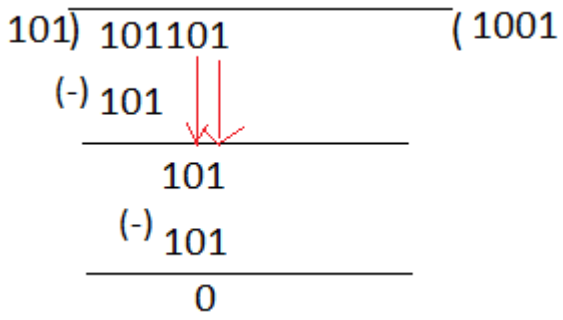
$$0 \times 0 = 0$$
$$1 \times 0 = 0$$
$$0 \times 1 = 0$$
$$1 \times 1 = 1 (\textit{there is no carry or borrow for this})$$

```
   1011.01
 ×   110.1
 -------
   101101
  0000000
 1011010
1011010000
-----------
1001001.001
```

Binary Division

Binary division is an important but often overlooked part of binary arithmetic. Though it is not too difficult, it may look a bit tougher than the other binary operations because all the other had some similarity among

themselves like they all had four basic steps which made all the processes quite easy to understand. But the process of binary **division** does not have any ***specific*** rules to follow.



LOGIC GATES AND BOOLEAN ALGEBRA

Boolean algebra or switching algebra is a system of mathematical logic to perform different mathematical operations in binary system. These are only two elements 1 and 0 by which all the mathematical operations are to be performed. There only three basis binary operations, AND, OR and NOT by which all simple as well as complex binary mathematical operations are to be done. There are many rules in Boolean algebra by whichthose mathematical operations are done. In Boolean algebra, the variables are represented by English Capital Letter like A, B, C etc and the value of each variable can be either 1 or 0, nothing else.

Some basic logical Boolean operations-
AND operation,

$$0.0 = 0$$
$$0.1 = 0$$
$$1.0 = 0$$
$$1.1 = 1$$

OR operation,

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

Not operation,

$$\overline{1} = 0$$
$$\overline{0} = 1$$

Some basic laws for Boolean Algebra,

$$\overline{0} = 1, \overline{1} = 0, \; if \; A = 1 \; then \; \overline{A} = 0 \; and \; if \; A = 0, \; then \; \overline{A} = 1.$$

A . 0 = 0 where A can be either 0 or 1.
A . 1 = A where A can be either 0 or 1.
A . A = A where A can be either 0 or 1.
A . Ā = 0 where A can be either 0 or 1.
A + 0 = A where A can be either 0 or 1.
A + 1 = 1 where A can be either 0 or 1.
A + Ā = 1
A + A = A
A + B = B + A where A and B can be either 0 or 1.

A . B = B . A where A and B can be either 0 or 1.
The laws of Boolean algebra are also true for more than two variables like,
Cumulative Laws for Boolean Algebra

$$A+B+C=A+C+B=B+A+C=B+C+A=C+A+B=C+B+A$$
$$A.B.C=A.C.B=B.A.C=B.C.A=C.A.B=C.B.A$$

Associative Laws for Boolean Algebra

$$(A+B)+C=A+(B+C)$$
$$(A.B).C=A.(B.C)$$

Distributive Laws for Boolean Algebra

$$A.(B+C)=A.B+A.C$$

Redundant Literal Rule

$$AA+\overline{A}A+AB+\overline{A}B$$

Rules of Boolean Algebra

$1.A+0=A$	$7.A \bullet A=A$
$2.A+1=1$	$8.A \bullet \overline{A}=0$
$3.A \bullet 0=0$	$9.\overline{\overline{A}}=A$
$4.A \bullet 1=A$	$10.A+AB=A$
$5.A+A=A$	$11.A+\overline{A}B=A+B$
$6.A+\overline{A}=1$	$12.(A+B)(A+C)=A+BC$

A, B, and C can represent a single variable or a combination of variables.

DE MORGAN'S THEREM,

$$\overline{A+B}=\overline{A}\,\overline{B}$$
$$and\ \ \overline{AB}=\overline{A}+\overline{B}$$

Proof from truth table,

Inputs		Outputs			
A	B	$\overline{A+B}$	$\overline{A}.\overline{B}$	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	0	0	1	1
1	0	0	0	1	1
1	1	0	0	0	0

$$Column\ for\ \overline{A+B}\ and\ \overline{A}.\overline{B}\ are\ same.$$

$$Column\ for\ \overline{AB}\ and\ \overline{A}+\overline{B}\ are\ same.$$

Examples of Boolean Algebra

$$Simplify,\ \overline{(A+\overline{B})(C+\overline{D})}$$

$$Here,\ \overline{(A+\overline{B})(C+\overline{D})}\ [\ As\ per\ De\ Morgan\ Therem\ \overline{x.y}=\overline{x}+\overline{y}\ ]$$

$$=\overline{(A+\overline{B})(C+\overline{D})}\ [\ As\ per\ De\ Morgan\ Therem\ \overline{x+y}=\overline{x}.\overline{y}\ ]$$

$$=\overline{A}.\overline{\overline{B}}+\overline{C}.\overline{\overline{D}}$$

$$=\overline{A}B+\overline{C}D$$

These are another method of simplifying complex Boolean expression. In this method we only use three simple steps.

1. Complement entire Boolean expression.
2. Change all ORs to ANDs and all ANDs to ORs.
3. Now, complement each of the variable and get final expression.

By this method,

$\overline{(A+\overline{B})(C+\overline{D})}$ will be first complemented, i.e. $(A+\overline{B})(C+\overline{D})$ .Now, change all (+) to (.) and (.) to (+) i.e. $A\overline{B}+C\overline{D}$. Now, complement each of the variable, $\overline{A}B+\overline{C}D$. This is the final simplified form of Boolean expression, $\overline{(A+\overline{B})(C+\overline{D})}$

And it is exactly equal to the results which have been come by applying De Morgan Theorem.

Another example,

$$\overline{\overline{AB}+\overline{A}+AB}=\overline{\overline{AB}}.\overline{\overline{A}}.\overline{\overline{AB}}\quad[Appling\ De\ Morgan\ Therem]$$

$$=AB.A.\overline{\overline{AB}}$$

$$=AB.\overline{\overline{AB}}.A=0$$

By Second Method,

$$\overline{\overline{AB}+\overline{A}+AB}=\overline{\overline{A+B}.\overline{A}.A+B}=(\overline{\overline{A}+\overline{B}}).A.(\overline{A}+\overline{B})=0$$

$$Example\ simplify,\ AB+A\overline{B}C+B\overline{C}=A(B+\overline{B}C)+B\overline{C}=A(B+\overline{B})(B+C)+B\overline{C}$$

$$=AB+AC+B\overline{C}=AB(C+\overline{C})+AC+B\overline{C}=ABC+AB\overline{C}+AC+B\overline{C}$$

$$=AC(1+B)+B\overline{C}(A+1)=AC+B\overline{C}$$

Representation of Boolean function in truth table.
Let us consider a Boolean function,

$$f(A,B,C) = \bar{A}B + \bar{B}C.$$

Now let us represent the function in truth table.

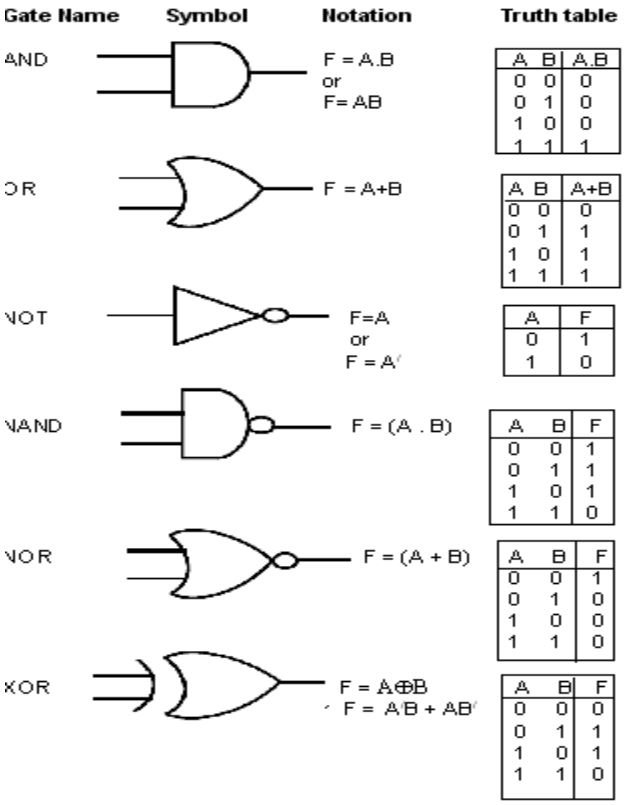
A	B	C	$\bar{A}B$	$\bar{B}C$	$\bar{A}B+\bar{B}C$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

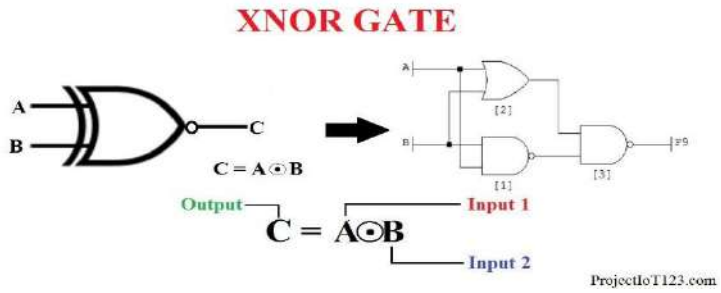
LOGIC GATES:

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a **certain logic**. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc. Logic gates are primarily implemented using diodes or transistors acting as electronic switches. **Logic circuits** include such devices as multiplexers, registers, arithmetic logic units (ALUs), and computer memory, all the way up through complete microprocessors, which may contain more than 100 million gates. In modern practice, most gates are made from MOSFETs (metal–oxide–semiconductor field-effect transistors).

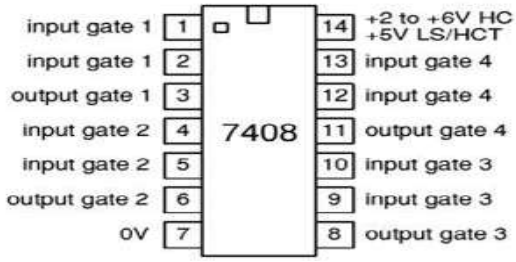
Compound logic gates AND-OR-Invert (AOI) and OR-AND-Invert (OAI) are often employed in circuit design because their construction using MOSFETs is simpler and more efficient than the sum of the individual gates.

LOGIC GATES AND THEIR TRUTH TABLES:





AND GATE IC (2 INPUT):EXAMPLE OF LOGIC GATE



BOOLEAN FUNCTION REPRESENTATION

The use of switching devices like transistors give rise to a special case of the Boolean algebra called as switching algebra. In switching algebra, all the variables assume one of the two values which are 0 and 1.In Boolean algebra, 0 is used to represent the 'open' state or 'false' state of logic gate. Similarly, 1 is used to represent the 'closed' state or 'true' state of logic gate. A Boolean expression is an expression which consists of variables, constants (0-false and 1-true) and logical operators which results in true or false. A Boolean function is an algebraic form of Boolean expression. A Boolean function of n-variables is represented by f(x1, x2, x3….xn). By using Boolean laws and theorems, we can simplify the Boolean functions of digital circuits. A brief note of different ways of representing a Boolean function is shown below.

- Sum-of-Products (SOP) Form
- Product-of-sums (POS) form
- Canonical forms

DOMAIN OF EXPRESSION:It is the set of variables present in that expression.

Sum of Product (SOP) Form

The sum-of-products (SOP) form is a method (or form) of simplifying the Boolean expressions of logic gates. In this SOP form of Boolean function representation, the variables are operated by AND (product) to form a product term and all these product terms are ORed (summed or added) together to get the final function. A sum-of-products form can be formed by adding (or summing) two or more product terms using a Boolean addition operation. Here the product terms are defined by using the AND operation and the sum term is defined by using OR operation. The sum-of-products form is also called as Disjunctive Normal Form as the product terms are ORed together and Disjunction operation is logical OR.

STANDARD SOP:A Standard SOP is the one in which all the variables in domain appear in each product term in expression.ex: A'BC + AB'C + ABC ' + ABC

Non standard SOP: AB + ABC + CDE

SOP form representation is most suitable to use them in FPGA (Field Programmable Gate Arrays).

Examples

AB + ABC + CDE

A'BC + AB'C + ABC' + ABC

SOP form can be obtained by

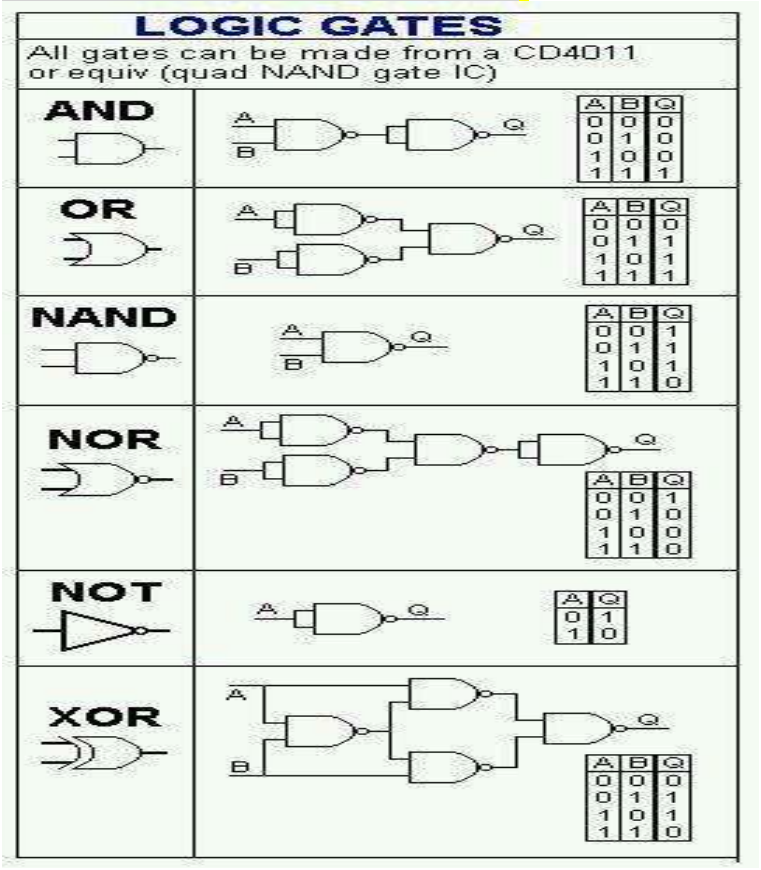
- Writing an AND term for each input combination, which produces HIGH output.
- Writing the input variables if the value is 1, and write the complement of the variable if its value is 0.
- OR the AND terms to obtain the output function.

Product of Sums (POS) Form

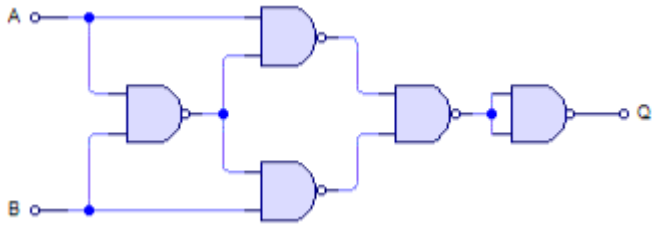
The product of sums form is a method (or form) of simplifying the Boolean expressions of logic gates. In this POS form, all the variables are ORed, i.e. written as sums to form sum terms. All these sum terms are ANDed (multiplied) together to get the product-of-sum form. This form is exactly opposite to the SOP form. So this can also be said as "Dual of SOP form". Here the sum terms are defined by using the OR operation and the product term is defined by using AND operation. When two or more sum terms are multiplied by a Boolean OR operation, the resultant output expression will be in the form of product-of-sums form or POS form. The product-of-sums form is also called as Conjunctive Normal Form as the sum terms are ANDed together and Conjunction operation is logical AND. Product-of-sums form is also called as Standard POS.
Examples :(A+B) (A + B + C) (C +D)**(NON Standard POS)**
(A + B + C) (A + B + C ') (A + B' + C) (A' + B + C)**(Standard POS)**

UNIVERSAL GATES-NAND AND NOR GATES:

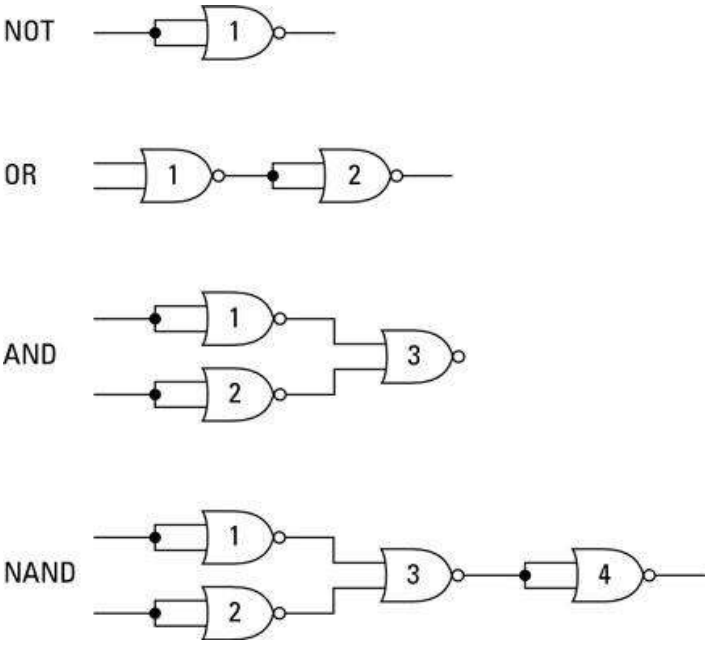
NAND GATE AS UNIVERSAL GATE:



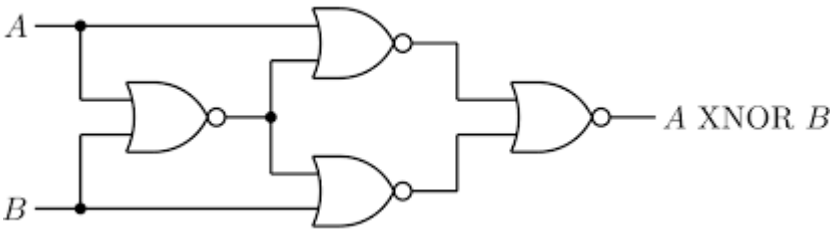
EXNOR GATE FROM NAND GATE



NOR GATE AS UNIVERSAL GATE:



EXNOR GATE FROM NOR GATE



EXOR GATE FROM NOR GATE